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The Application of Low Energy Scanning-Transmission Electron Microscopy (LVSTEM) to the Study of Semiconductor Materials and Devices

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While the Scanning Transmission Electron Microscope was introduced some 40 years ago by Crewe et al, its application at low beam energies has been rather limited. There are several reasons for this, including a traditional separation of the SEM, TEM, and STEM communities. Other important factors include the difficulty of thin sample fabrication, and the general interest of the STEM community in the use of very advanced tools with probe diameters in the range of 1.0 to 0.1nm.

However, recent publications by Hitachi [1], Dunne [2], coupled with the high-speed production of thin samples by FIB, have demonstrated the exceptional promise of LVSTEM for semiconductor device examination. Indeed, it is likely that low voltage STEM (LVSTEM) will replace traditional "mechanically polished" cross sections in the next three years. There are compelling reasons driving this transition, including sub-micron positioning accuracy, no charging, no chemical etching and finally, and most importantly, increased layer contrast promoted by low energy operation.

The present study reports on our initial results using FIB-prepared semiconductor devices examined in a Hitachi S5200 UHR SEM with the addition of a "dedicated" STEM imaging aperture, transmitted electron detector with supporting electronics, and operation software. The instrument was not modified in any other way to enable STEM operation. This was a "field retrofit" and was accomplished in one day. Figures 1 shows the STEM sample holder used in this work.

One advantage of this electron optic configuration is that the instrument can be operated as a "conventional" SEM at very low magnifications (30X). This greatly facilitates the location of the pre-thinned region of the STEM sample. Additionally, high-resolution SEM images are possible on very flat, FIB-prepared samples using the secondary detector. The thin sample geometry, coupled with the in-lens detector, promotes the formation of SEM images with high SE1 content. Figures 2a and 2b, show corresponding SEM and STEM images of tungsten plug/transistor structures.

Figure 3a shows an example from our early LVSTEM studies. With comparable resolution to the conventional 200kV TEM image as seen in figure 3b, we observe excellent contrast between the polysilicon gate electrode and the SiO2 spacer liner. In dark contrast is the SiN spacer itself. The strong contrast between the SiO2 and the SiN is somewhat unexpected considering their modest density difference (2.2 vs 3.2 g/cm3). The image quality, while better in the CTEM image, is still comparable between the two techniques. The combination of FIB prepared thin foils and STEM imaging in a UHR SEM, provide a compelling imaging solution for advanced CMOS transistor development.

References

[1] Hitachi High-Technologies, Technical Data, SEM 100.
[2] M. Nakagawa and R Dunne, Journal of the Japanese Society for EM, 51(1), 53-57 (2002).

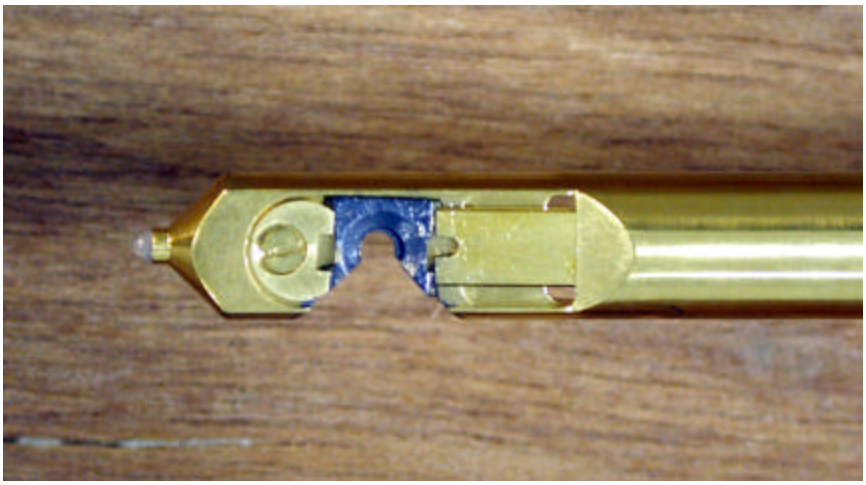

Figure 1 STEM sample holder

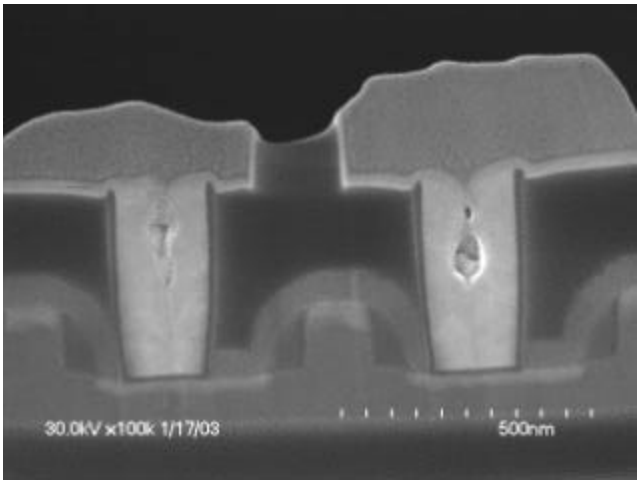

Figure 2a 30kV SEM of plugs and transistors

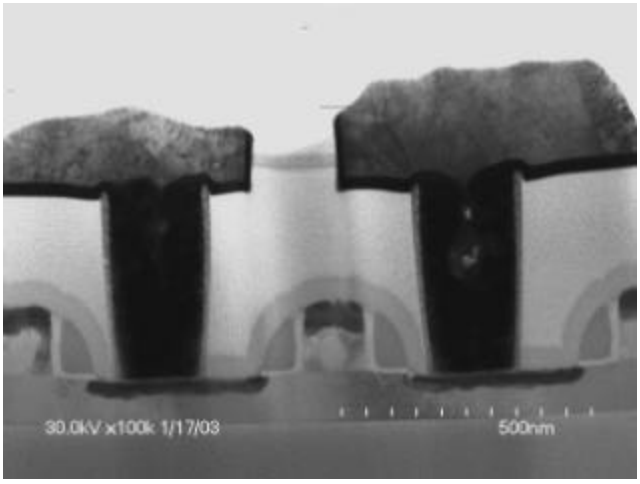

Figure 2b corresponding 30kV STEM image

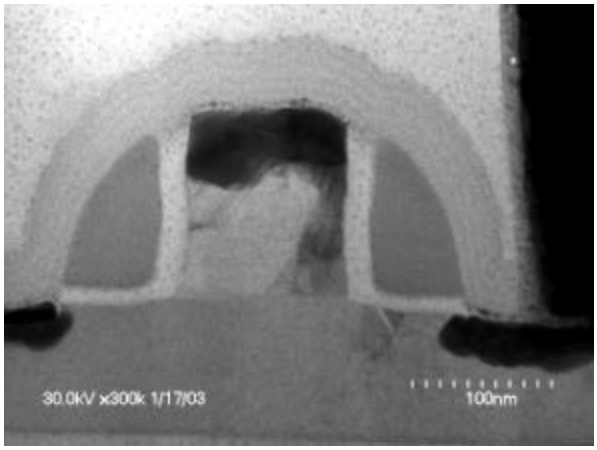

Figure 3a 30kV STEM image of transistor

Figure 3b corresponding 200kV TEM image

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