Dual Lens Electron Holography, Scanning Capacitance Microscopy (SCM), Scanning Spreading Resistance Microscopy (SSRM) Comparison for Semiconductor 2-D Junction Characterization

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Abstract: 2-D junction characterization by dual lens electron holography, scanning capacitance microscopy (SCM), and scanning spreading resistance microscopy (SSRM) on a variety of semiconductor devices is reported, including optical modulators, regular complementary metal-oxide-semiconductor (CMOS) devices, and SiGe hetero-junction bipolar transistors. In most cases these techniques provide comparable results, while in some instances one technique has advantages over the other and vice versa. Advantages and disadvantages of each technique are discussed.

Keywords: Dual lens electron holography, scanning capacitance microscopy (SCM), scanning spreading resistance microscopy (SSRM), 2-D junction profile, SiGe hetero-junction bipolar transistor (HBT)

Introduction

Junction profiling at the microscopic scale is a critical part of characterization for semiconductor development and manufacturing. Over the years, the accuracy and repeatability of semiconductor junction profiling techniques have been improved significantly, especially electron holography, scanning capacitance microscopy (SCM), and scanning spreading resistance microscopy (SSRM). However, the potential of these junction profiling techniques has not yet been fully realized and well publicized in the semiconductor industry.

In this paper, we provide a review of a few examples illustrating how these techniques compare in the junction characterization of semiconductor devices and discuss their common features and differences. Although the techniques address two-dimensional (2-D) junction characterization in semiconductor devices, they measure different types of physical properties of the semiconductor material. Holography measures electrostatic potential due to carrier concentration variation and is a bulk measurement technique; SCM measures carrier type and concentration and is a near surface technique; and SSRM measures local spreading resistance and is also a near surface technique. These techniques provide complementary results of active dopant distribution in a semiconductor sample. In general, electron holography can achieve higher spatial resolution compared to SCM and SSRM. Electron holography requires thick samples for sensitivity, whereas SCM is more sensitive to surface active dopant and does not require thick samples. Overall, these techniques provide comparable results with minor differences. Depending on the application, one technique has an advantage over the other.

Theoretical Background

Electron holography. Electron holography measurements are performed using a transmission electron microscope (TEM). Here, electrostatic potential is determined by measuring the phase difference between electron beams passing through n-doped and p-doped regions of the semiconductor devices [1–14]. A schematic of an electron holography setup is shown in Figure 1a, where an electron beam passing through the sample interferes with the reference beam passing through a nearby vacuum and forms interference fringes over the image of the sample. Figure 1b shows a phase shift of the fringe where holography fringes are overlaid on top of different types of semiconductor: n-type or p-type. Fourier transform on the holographic image is used to obtain an image in reciprocal space where one of the two sidebands is selected, and the main beam is masked off. An inverse Fourier transform on one of the selected sidebands is performed to obtain phase and amplitude maps [9,10]. The amplitude image is similar to a regular TEM image, while the phase image can only be measured through the interference imaging method. The phase shift is proportional to the electrostatic potential. Based on the theoretical calculations for Si at room temperature shown in Figure 2, the electrostatic potential varies linearly with the active dopant concentration [15].

Dual lens electron holography. In general, meaningful semiconductor junction mapping by electron holography requires the following: (1) a fringe width (fringe overlap) in the range of about 100 to 800 nm for an adequate field of view (FOV); (2) fringe spacing between 0.2 and 10 nm for meaningful spatial resolution; (3) visibility of the fringe contrast (10–30%) for useful signal-to-noise ratio; and (4) adjustability of both the field of view and the fringe spacing relative to the sample.

In previous papers and a patent disclosure, we reported a dual lens electron holography method that meets the above requirements [2–6]. The dual lens operation allows electron holography to be performed from low to high magnification and provides the field of view and fringe spacing necessary for 2-D junction profiling in devices with various sizes.

Figure 3 summarizes the results for fringe width and fringe spacing relative to the objective lens excitation from a FEI Titan TEM on which dual lens electron holography was implemented. The results show the achieved range of values for FOV and fringe spacing necessary for semiconductor device characterization. The fringe spacing decreases from 4 nm

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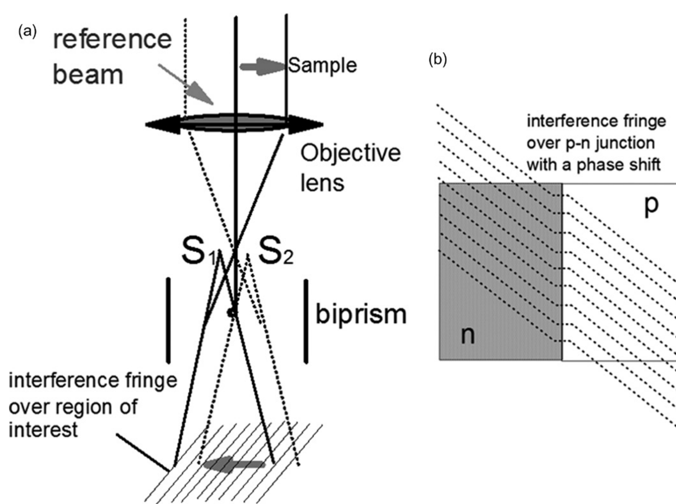


Figure 1: (a) Diagram of electron holography; (b) interference fringes overlay on top of n-type and p-type Si with a phase shift between.

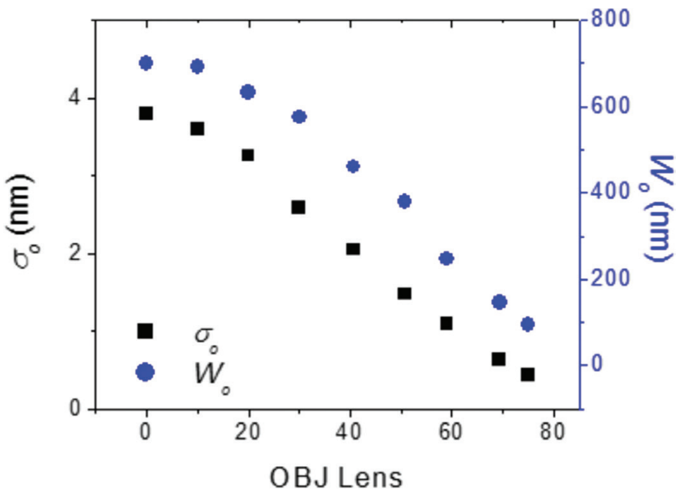
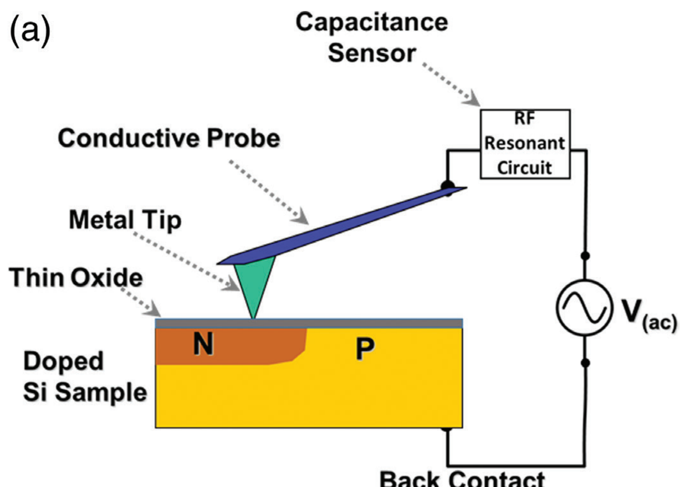


Figure 3: Fringe spacing and fringe width versus first objective current for a FEI Titan instrument. The fringe spacing relative to the object is on the left axis, and fringe width is on the right axis.

to 0.2 nm; while the field of view is reduced from 700 nm to 100 nm when the first objective lens current increases with a constant biprism voltage, and the second objective lens is adjusted to refocus the image back to the same imaging plane. With a constant biprism voltage, the contrast varies slightly through the dual lens operational ranges [2,5].

For the current experiments, dual lens electron holography was performed with 200 KeV beam energy. TEM samples were prepared by delayering from the top close to the region of interest with less than 100 nm material remaining just above the Si surface. A sample was either polished to 200–300 nm thickness or prepared by focused ion beam (FIB) milling to about 400 nm thickness. All samples were coated with carbon on both sides of a TEM sample to avoid charging.

Scanning capacitance microscopy (SCM). SCM is a 2-D p/n junction profiling technique used for mapping active dopant distribution on semiconductor surfaces [16]. It utilizes a modified atomic force microscope (AFM) by employing a conductive probe tip with one end attached to a capacitance sensor, as shown in Figure 4a, while the other



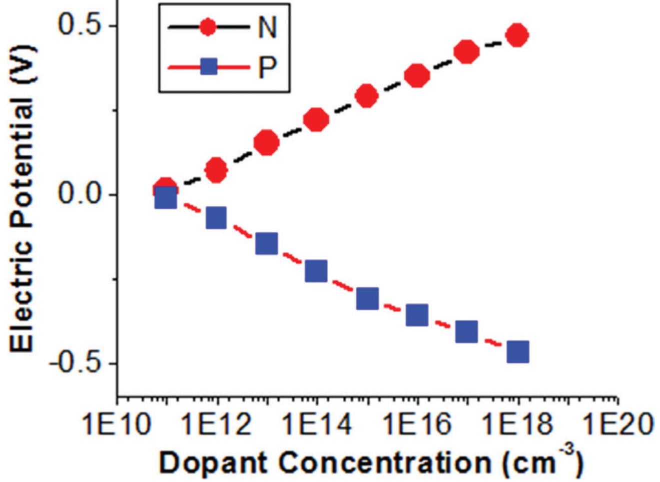


Figure 2: Electrostatic potential versus dopant concentration at T=300°K.

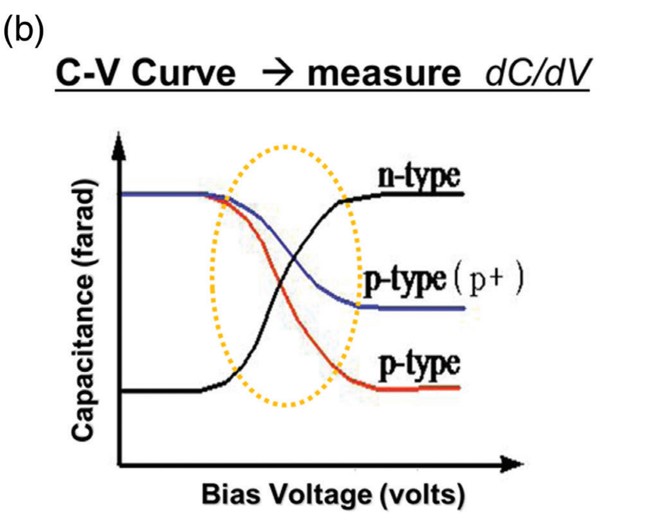


Figure 4: (a) Schematic of SCM; (b) electric curve of SCM.

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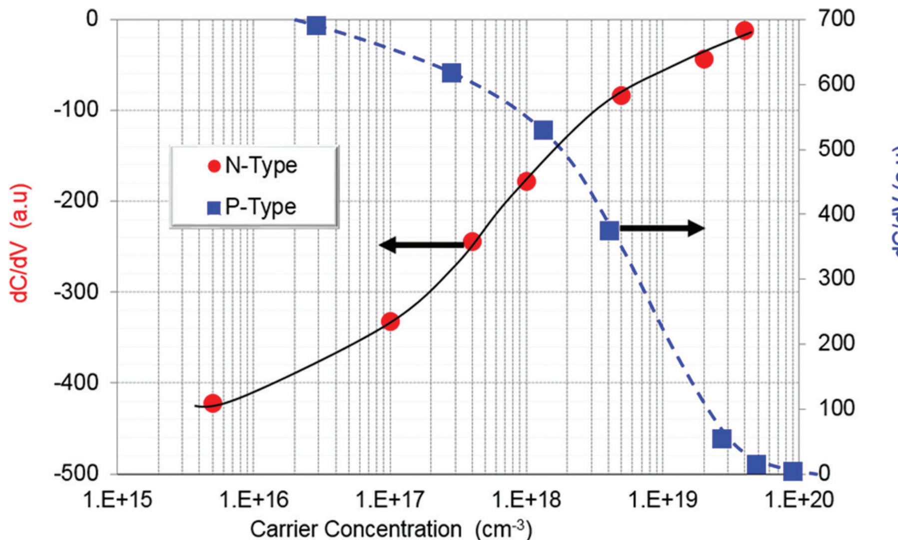

Figure 5: SCM differential capacitance (*dC/dV*) versus active dopant concentration on n-type and p-type staircase samples.

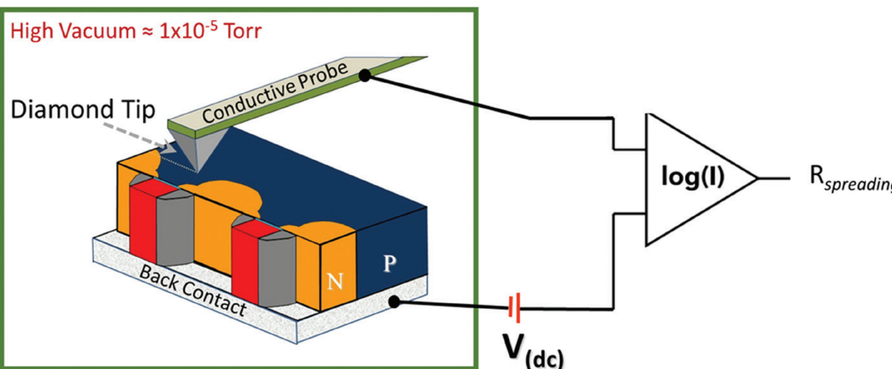

Figure 6: SSRM setup showing the required high vacuum, common back contact, MOS device cross section to be imaged, diamond probe tip, DC bias and logarithmic current amplifier, and spreading resistance relation to active dopant density.

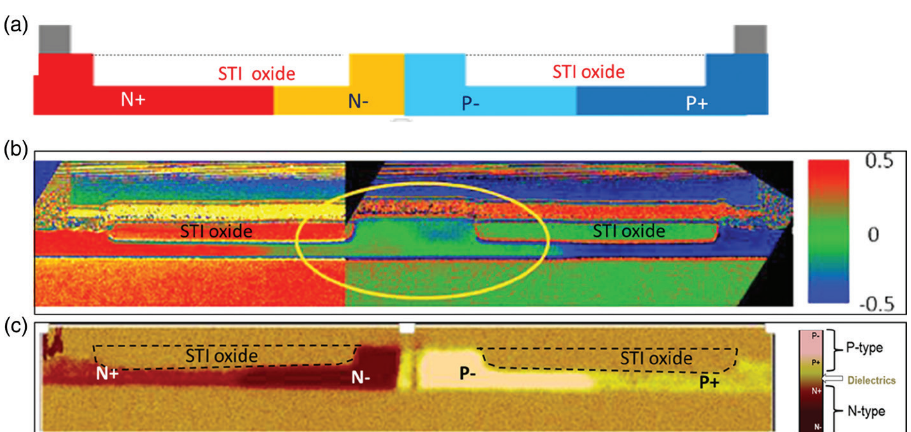

Figure 7: (a) Schematics of an optical modulator; (b) phase map by electron holography; (c) differential capacitance (*dC/dV*) map by SCM.

end has a sharp tip used to scan a sample surface that is coated with a thin oxide layer. An AC bias is applied to the sample with respect to the probe tip, thereby forming a metal-oxide-semiconductor (MOS) capacitor structure. During each cycle of the AC bias, the majority carriers in the semiconductor sample undergo localized depletion and accumulation directly below the SCM tip, thereby generating a capacitance-voltage (CV) curve as illustrated in Figure 4b. The magnitude of the slope of the CV curve in the depletion mode and its polarity are determined by the concentration and type of majority carriers in the vicinity of the tip contact, respectively. The SCM technique measures differential capacitance with respect to the bias voltage (*dC/dV*) as the tip is raster scanned across the sample surface. The phase of the signal represents the type of carriers, and its magnitude represents the concentration of carriers. Figure 5 shows the relationship between active carrier concentration with *dC/dV*. Here, a positive *dC/dV* indicates p-type carriers, and negative indicates n-type carriers. The SCM tip is scanned across the sample surface and allows mapping spatially resolved images of carrier types and concentration with high spatial resolution (~5 nm). Spatial resolution depends on tip dimension and geometry.

Although SCM is ideal for p/n junction delineation, the technique's sensitivity at high carrier concentration (>10^{20}cm^{-3}) is lower, and quantitative analysis is challenging. The SCM response within the depletion of a p/n junction depends on imaging parameters including AC and DC sample bias, as well as relative dopant concentration between the p and n sides. A typical p/n junction is characterized by a double inversion layer within the depletion zone. This feature has been reported [17] and is attributed to the space charge density described in an ideal p/n junction [18].

Scanning spreading resistance microscopy (SSRM). Much like SCM, SSRM is an AFM-based technique that is used for mapping active dopant distribution on semiconductor surfaces. It uses a conductive probe tip that is scanned over a sample surface while a DC bias is applied to the sample with respect to the tip [19]. The experimental setup for SSRM, shown in Figure 6, requires an inert or

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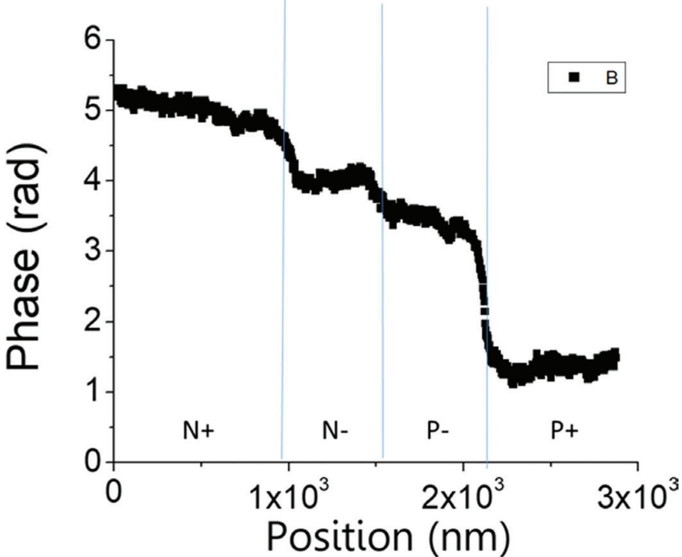

Figure 8: Line profile of junction from left to right in Si of Figure 7b.

vacuum environment to prevent surface oxidation and a hard material (diamond) tip to allow high-pressure contact and thereby measure spreading resistance that directly correlates to active dopant concentration. By conducting these measurements in a high-vacuum environment (10^{-5} Torr), the sample surface oxidation and water vapor are minimized. Vacuum SSRM allows reduction of the minimum pressure required to achieve spreading resistance mode imaging and, therefore, improved spatial resolution and good repeatability of results. Figure 6 also shows the required back contact to all regions to be imaged. Sample preparation methods have been developed to ensure that low-resistance ohmic back contact is formed for all regions of interest. The typical spatial resolution of SSRM is ~2 nm.

To perform SSRM measurements, high-contact pressure is applied between a degenerately doped diamond tip and a sample surface. For silicon samples, high pressure (>8 GPa) causes the Si crystal structure to undergo a local phase transformation from diamond to a beta-tin phase in which the band gap collapses to zero, therefore forming an ohmic contact between the tip and sample. The measured current is used to calculate the local spreading resistance at the tip-sample contact interface. The spreading resistance (R*sp*) varies with the local active doping concentration according to equation (1):

$$R_{sp} = \frac{1}{q\mu N \cdot 4 \cdot a} \quad (1)$$

where ***N*** is the active dopant concentration in the sample near the tip contact, ***a*** is the tip contact radius, ***q*** is electron charge, and ***μ*** is the majority carrier mobility [20].

Experimental Results

Electron holography and SCM junction profiles of an optical modulator. An optical modulator is a critical part of Si photonics circuitry, where properties of light propagating through a waveguide are modified to convert from a continuous beam to pockets of optical signals [21,22]. One example of the modulator design is a lightly doped p/n junction that connects with highly doped n+ and p+ on the left and right side for contact, shown in Figure 7a. Since this device has n+, n-, p-, and p+ dopant at close vicinity, it is an ideal device to study the variation of electrostatic potential and differential capacitance with active dopant concentration using electron holography and SCM. Figure 7b is an electrostatic potential map (phase map) measured by electron holography: the right side is the p+ dopant contact with approximately a one-rad phase shift, and the left side is the n+ dopant contact with a five-rad phase shift, shown as a line profile in Figure 8. The middle section, which is indicated by the circled region in Figure 7b, is the optical modulator p/n junction with a smaller phase shift difference between n- and p-. The phase shift steps down from left to right with n+, n-, p-, and p+ as dopant concentration changes, which is consistent with the plot of the electrostatic potential versus dopant concentration shown in Figure 2. Ideally, if calibrated, the active dopant concentration can be measured.

Figure 7c is the differential capacitance (*dC/dV*) map (amplitude and phase) by SCM: the extreme right is the p+ doped contact, and the extreme left is the n+ dopant contact. The middle portion is an optical waveguide formed with a lower doped p/n junction, which forms an optical modulator. A 1-D profile through the modulator structure in Figure 9 shows opposite polarity signals in n versus p doped Si, low-signal intensity in highly doped n+ and p+ regions, and high intensity in n- and p- regions. The p/n junction is observed as a signal swing between positive and negative.

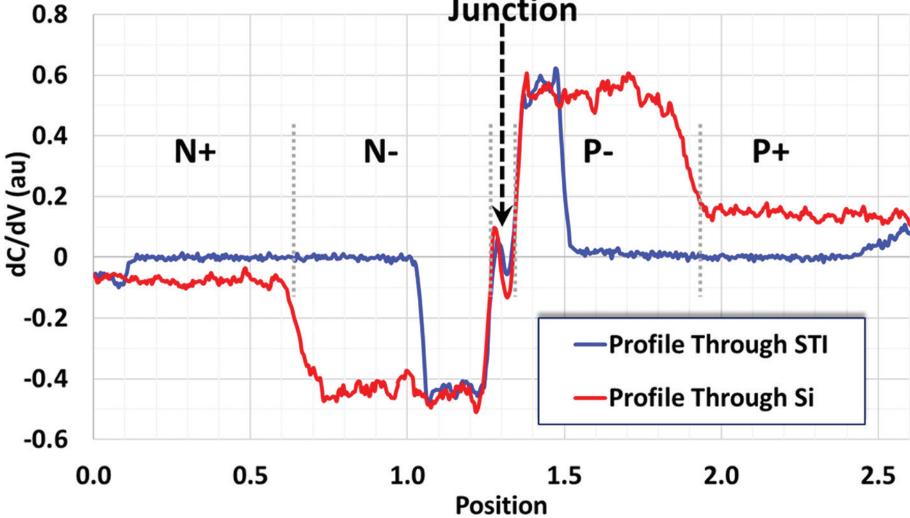

Figure 9: Lateral line profiles of carrier type and concentration taken through STI (shallow trench isolation) and Si in Figure 7c.

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A comparison of the 2-D maps shown in Figures 7b and 7c, as well as 1-D profiles shown in Figures 8 and 9, demonstrate a qualitative agreement between SCM and electron holography. Both line profiles provide clear delineation of the p/n junction, as well as good contrast of dopant concentration and type. A minor difference at the P- region of the waveguide is observed. The electron holography map (Figure 7b) shows a slight shift toward n-type electrostatic potential at the bottom part of the P- region of the waveguide, while no shift is observed in the SCM map (Figure 7c) at the same location. This shift observed in electron holography could be due to charge at the bottom interface between Si/SiO_2.

Holography junction profiles of a negative field-effect transistor (NFET) device with <100> channel orientation. In a regular complementary metal-oxide-semiconductor (CMOS), the channel direction is normally along the <110> direction. However, based on band structure calculation, a higher p-FET drive current exists (high mobility) along the <100>. Therefore, in some applications, the <100> junction of Si is used. Because of that, the junction profile for a <100> channel device is of interest in semiconductor development and manufacturing. The advantage of analyzing a <100> channel device is that the tilt angle to off-zone in the TEM is quite small, ~0.2°, compared to >1–2° angle required for analyzing a <110> channel device. This allows reduction of the projection effects in junction profile imaging due to sample tilt. Therefore, high spatial resolution in the junction profile is achievable.

Figure 10 shows a junction profile for a NFET where n-type source-drains and source/drain extension (SDE) regions are represented by red; p-type channel and p-well regions are represented by blue and green, respectively. In the map, the slightly blue color just below the gate indicates that the region has higher p-type active dopant concentration than the green region near the bottom edge of the image. The overlap of n-type SDE with the gate is clearly visible. SDE overlap with the gate provides the critical overlap capacitance (COV) necessary for optimum n-type metal-oxide-semiconductor (NMOS) device operation. Too much overlap leads to devices with source-drain (SD) leakage, and no overlap leads to a higher threshold voltage and lower drive current. Optimizing COV is critical for semiconductor device performance and manufacturing yield.

SSRM junction profile measurements of a positive field-effect transistor (PFET) device. High spatial resolution 2-D junction mapping of a PFET device fabricated in silicon-on-insulator (SOI) is discussed in [20]. Figure 11a shows a dark-field scanning transmission electron microscope (STEM) image of a PFET device with embedded-SiGe (eSiGe) in the source and drain regions. Two layers of e-SiGe, shown as light contrast in the image, consist of a thinner U-shaped buffer and the main SiGe layer that fills the U-shaped buffer layer. A channel SiGe (c-SiGe) layer used for work function adjustment is shown as a lighter contrast under the gate. The buried oxide is shown as a dark region along the bottom of the image. Figure 11b shows a spreading resistance image, with brown representing lower resistance, whereas yellow represents higher resistance regions. Low resistances are observed in the deep p+ source/drain, SDE (source-drain extension), NiSi contact regions, and gate stack. The dashed line illustrates the junction boundary between p+ SD, SDE, and n-well. In Si and SiGe regions, high resistance represents low carrier concentrations,

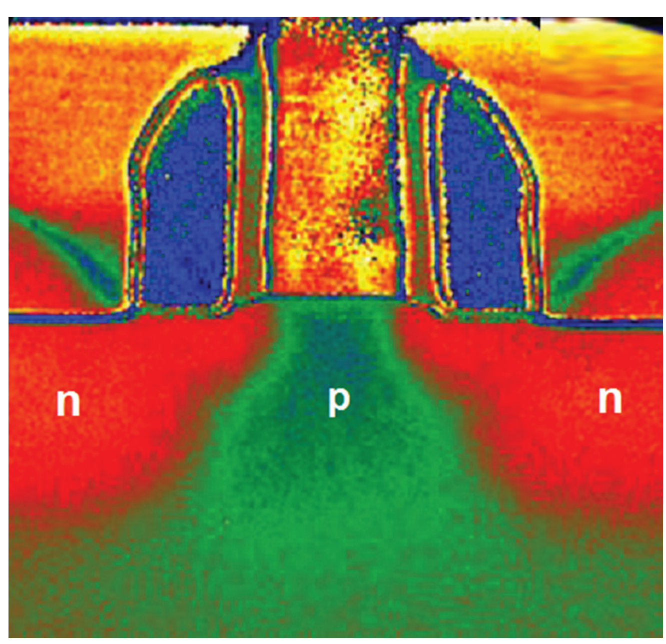
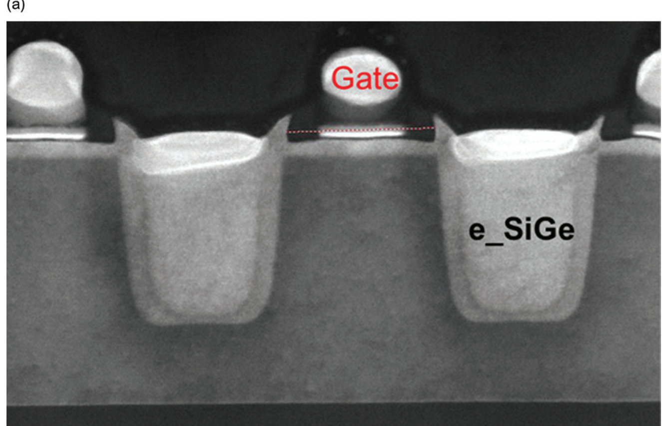


Figure 10: Junction profile of a <100> orientation complementary metal-oxide-semiconductor (CMOS) NFET device with 1 nm fringe spacing.

(a)



(b)

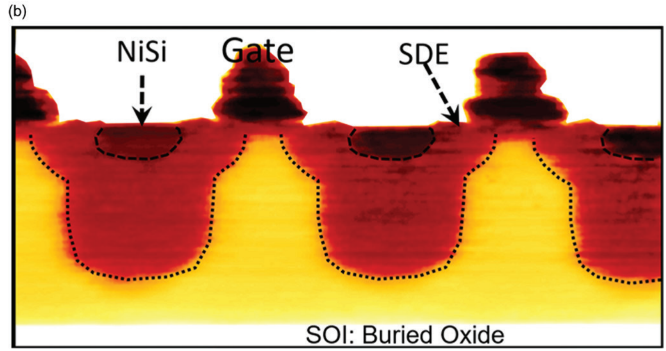


Figure 11: (a) Dark field STEM image showing e-SiGe and c-SiGe 22 nm SOI PFET devices; (b) spreading resistance image shows p+ deep SD, SDE, NiSi and gate in brown color that represent lower resistance, and low-doped n-Well in yellow color to represent higher resistance.

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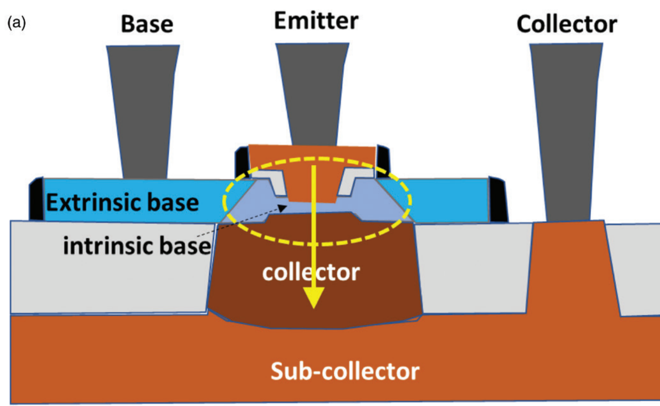
while low resistance represents high carrier concentrations (p type carrier). The buffer SiGe layer is initially undoped to limit boron diffusion into the device body. The buffer layer thins down near the SOI surface. The device was processed with a lower-dose boron implant to form SDE. The SSRM image (Figure 11b) clearly shows the SDE junction profile, including its overlap with the gate to form the required overlap capacitance for optimum device operation. Careful alignment of the STEM with SSRM image shows that the SD junction profile is outside of the buffer layer, indicating that boron diffused through it. This highlights that control of the thermal budget through the process is critical to control of dopant diffusion for optimum device performance. The dark layer under the gate in the SSRM image corresponds to the c-SiGe layer in the corresponding STEM image. The resistance contrast indicates that c-SiGe has a lower resistance compared to the underlying high resistance of Si n-well and remains doped n-type. Although the SSRM measures carrier profiles in semiconductors, the technique does not distinguish between n-type and p-type regions.

SiGe hetero-junction bipolar transistor (HBT). SiGe bipolar devices have been developed for high-frequency applications, such as mass-market low-cost radar systems for the automotive and drone industries [23]. To achieve high-speed performance, HBTs incorporate SiGe as a base region material with a n-p-n junction width of approximately 50 nm. Optimization of HBT device performance requires high spatial resolution mapping of the junction profiles and electrostatic potential in the junction. Figure 12 shows schematic drawings of SiGe bipolar devices. Figure 12a shows the overall structure of a HBT including the emitter, base, and collector. Figure 12b shows a close-up schematic of the SiGe hetero-junction region highlighted with a yellow dashed oval in Figure 12a.

Figure 13a is a 2-D map showing carrier and junction profiles of a HBT device by SCM analysis. The image shows, from top to bottom, n++ emitter, p-type SiGe base, n- collector, and n+ sub-collector. Figure 13b is the vertical 1-D carrier profile taken from the emitter to sub-collector along the center of the region, as illustrated with the yellow arrow in Figure 12b. At



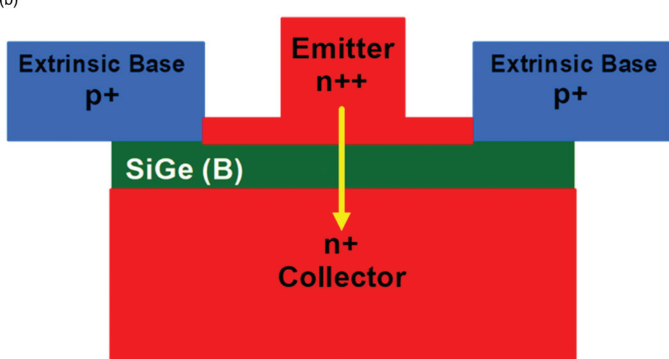
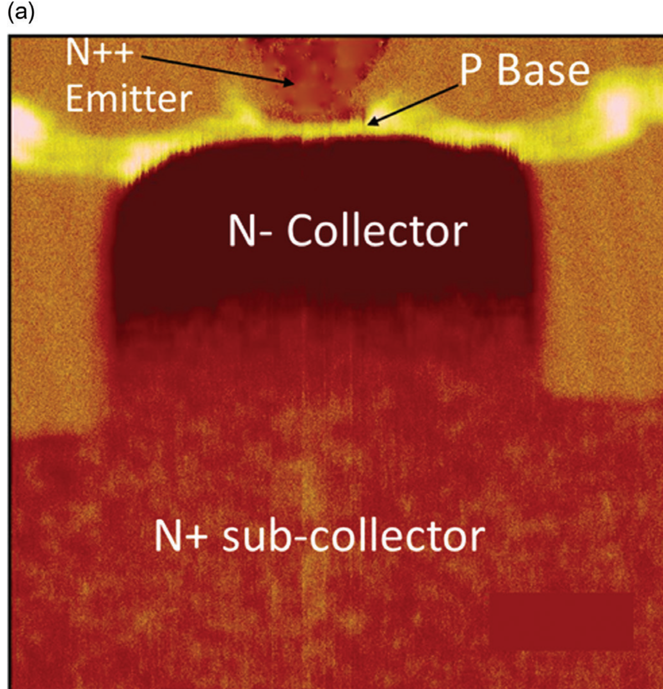


Figure 12: (a) Diagram of a hetero-junction bipolar transistor (HBT); (b) enlarged region of the dashed yellow oval region in Figure 12a with p-type SiGe hetero-junction doped with boron.



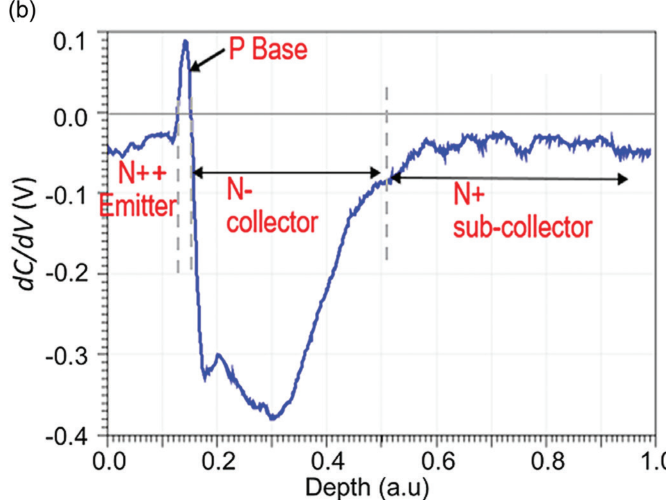


Figure 13: (a) SCM map of a hetero-junction bipolar transistor (HBT); (b) 1-D carrier depth profile through emitter-base-collector junctions in Figure 13a, also illustrated with a yellow arrow in Figure 12a.

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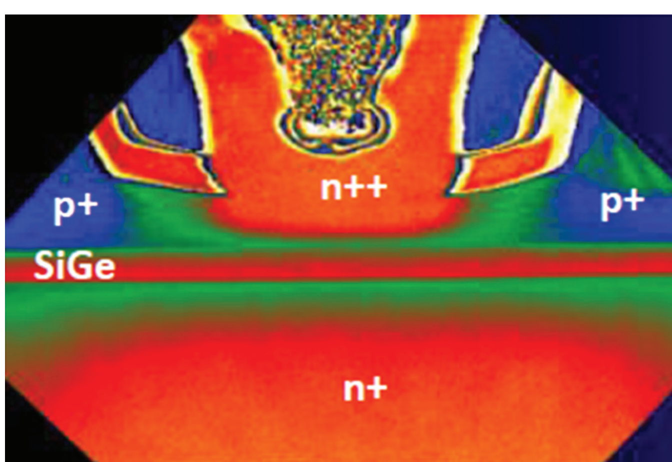

Figure 14: High spatial resolution junction mapping by electron holography for a bipolar SiGe device with 0.2 nm fringe spacing.

the extreme left, the profile shows a negative *dC/dV* signal with low intensity that indicates a highly doped n+ emitter. The signal is positive in the base region indicating a p-type carrier. The collector and sub-collector regions have negative *dC/dV* signals with high and low intensities indicating n- and n+ doping, respectively.

Figure 14 is a junction map of a bipolar SiGe device with 0.2 nm fringe spacing by dual lens electron holography. The middle red layer is the SiGe layer with electrostatic potential different from the Si material. Figure 15 is the junction line profile of Figure 14 from top to bottom, with the line profile position shown as the yellow arrow in Figure 12b. In the line profile (Figure 15), the SiGe layer is the p-type material sandwiched between n++ on top and n+ at the bottom, with the top part as the emitter, followed by the SiGe layer as the p-type base in the middle, and the bottom part as the collector. If we assume spatial resolution is 3× fringe spacing, the spatial resolution of Figure 14 is approximately 0.6 nm for the junction profile.

To obtain higher spatial resolution along the vertical line, Si is tilted along the horizontal direction until a white Si image is observed in order to get an electrostatic potential map in the region of interest without diffraction contrast. Therefore, there is no overlap or projection issue along the vertical direction of Figure 14. In the top of the emitter, the electrostatic potential of n++ is fully saturated toward the bottom of the conduction band (highest in electrostatic potential), while the blue p+ region on the two sides of the base contact is at the top of the valence band (lowest in electrostatic potential). Assuming the electrostatic potential difference of these two regions is approximately 1.1 V, and using these two regions of electrostatic potential, one can determine the location of the middle point in the bipolar device along the vertical direction.

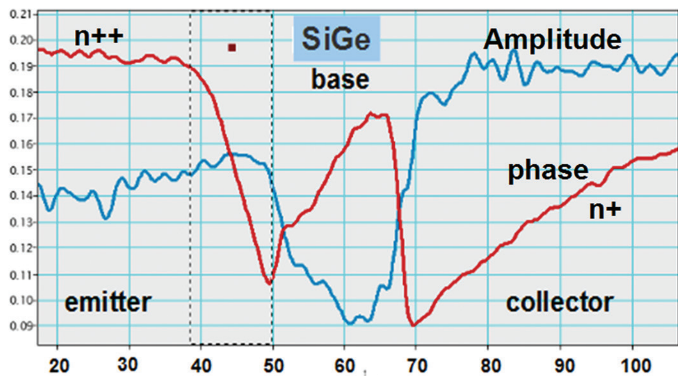

Figure 15: Vertical line profile of junction profile in Figure 14 from top to bottom as a red curve. The blue curve is the amplitude intensity profile. The line profile position is shown in Figure 12b as the yellow arrow.

In the electron holography measurement, the electrostatic potential of the p-type SiGe is different from the p-type Si. In this case, the p-type SiGe shows as red in Figure 14, which is similar in color to the n-type Si. In contrast, the SCM measurement is sensitive to carrier type and concentration, but it does not distinguish the material type as Si and SiGe as shown in Figure 13a. In this case the thin layer p-type SiGe in the middle of the device has a similar *dC/dV* value as the one for the p-type Si on the side (bright white color). It is noted that the device in Figure 13 has a wider n- region than that shown in Figure 14. This difference is due to different manufacturing conditions for the two devices.

The electrostatic potential in SiGe, shown as a red curve in Figure 15, is a function of Ge concentration. The amplitude profile (blue curve) shows that the SiGe layer has lower amplitude despite a higher Ge concentration, an opposite behavior to the electrostatic potential measurement. The signal-to-noise ratio is lower in amplitude profile compared to the phase profile. This indicates that the electrostatic potential profile is more sensitive to Ge concentration variation than the amplitude profile. It has been reported that Ge concentration variation within the SiGe layer can greatly enhance device speed [23]. However, the phase profile is the convolution of electrostatic potential of SiGe and carrier concentration. To accurately measure Ge concentration variation in such a thin layer structure, dark field electron holography with high spatial resolution can be used to measure the lattice constant along the vertical direction [12,13]. The larger the lattice constant, the higher the Ge concentration. This kind of Ge concentration variation characterization in SiGe layers is critical for process development, process matching, and physical defect analysis.

Discussion

The examples presented in this paper show that dual lens electron holography enables high spatial resolution junction mapping with good signal-to-noise ratio for various applications. Dual lens electron holography can obtain the highest spatial resolution of 0.6 nm with fringe spacing of 0.2 nm (under the assumption that spatial resolution of an electron hologram is 3× fringe spacing). More industrial applications of the technique have been published [24–26].

One limiting factor to the spatial resolution for electron holography is the sample tilt, which causes projection issues. For junction profile analysis, the sample is tilted off zone axis to reduce the diffraction contrast in the sample to obtain an electrostatic potential image. Depending on the tilt and sample

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thickness, this effect may result in junction smear to about 1–2 nm. SCM and SSRM, however, do not have this limitation, and they are surface sensitive techniques with typical spatial resolution of 5 nm and 2 nm, respectively.

Conclusion

High spatial resolution electron holography enabled by a dual lens system is a valuable characterization technique for semiconductor devices, but the sample thickness requirement limits its application to certain types of devices. However, SCM does not have this limitation but has lower spatial resolution. SCM is well suited for p-n junction delineation and is sensitive to carrier concentrations in the range 10^{16}–10^{20} cm^{-3}. Electron holography is less sensitive in the low-dose region. Electrostatic potential from electron holography can be simulated directly with technology computer-aided design (TCAD) modeling. SSRM detects metallurgical junctions; its sensitivity to carrier concentrations is in the range 10^{15}–10^{21} cm^{-3} and provides higher spatial resolution than SCM but does not distinguish between n or p type carriers. Although no quantification was presented in this paper, spreading resistance measurements can be converted to absolute carrier concentration by using SSRM data captured from known calibration samples.

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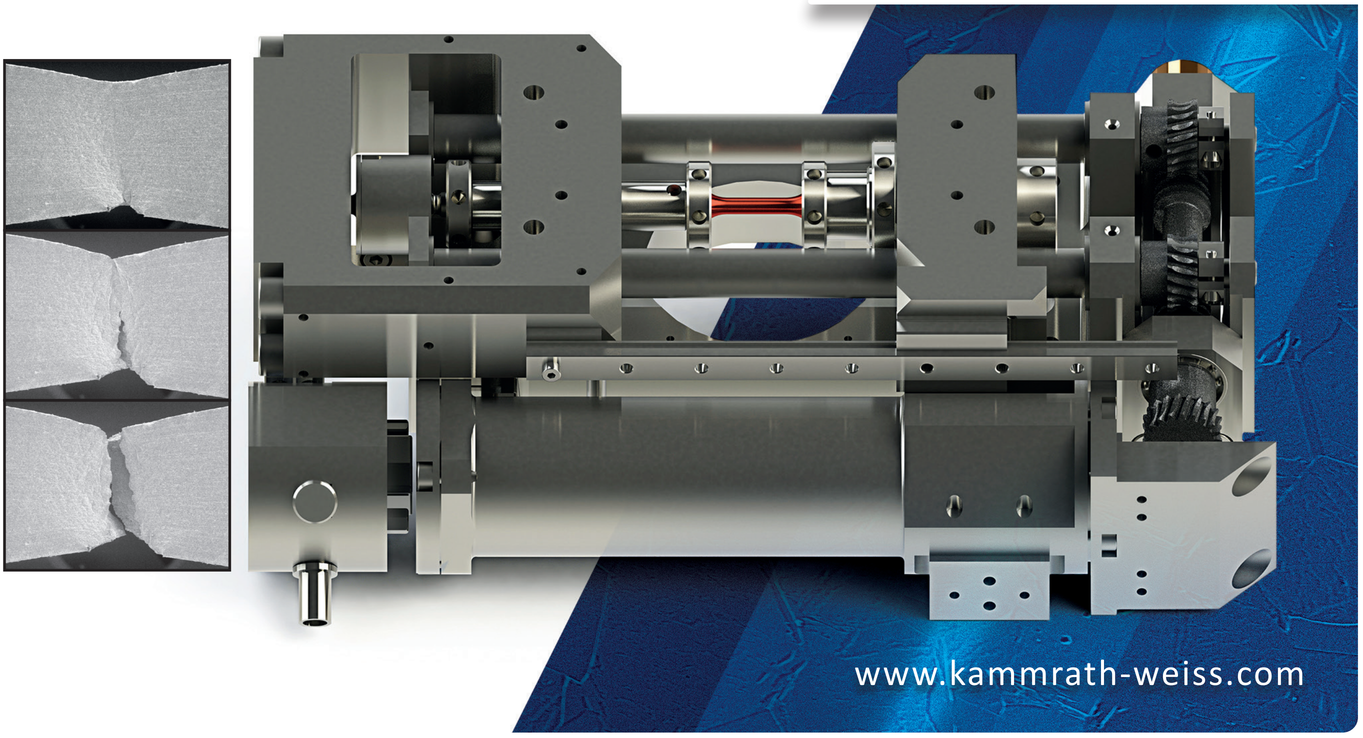

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