Microsc. Microanal. 21 (Suppl 3), 2015
doi:10.1017/S1431927615012441 Paper No. 1165


# Challenges and Opportunities in 3D Tri-gate Transistor Characterization

Jiong Zhang[1], Ling Pan[1], Andrew A. Herzing[2], Ray Twesten[3], Paolo Longo[3], Noel Franco[1], Kevin Johnson[1] and Zhiyong Ma[1]
[1.] Intel Corporation, Corporate Quality Network, Hillsboro, OR 97124
[2.] National Institute of Standards and Technology, Material Measurement Laboratory, Gaithersburg, MD 20899 USA
[3.] Gatan Inc., Pleasanton, CA 94588

Dimensional scaling has provided performance improvement and power reduction in the era of traditional MOSFET scaling. In the past decade, transistor performance has progressed through the introduction of innovations including strained silicon, high-k/metal gate, and novel architectures. Multi-gate devices have long held the promise of improved transistor electro-statics, offering improved performance at lower supply voltages and significantly reduced short channel effects [1]. Intel has deployed fundamentally different 3D tri-gate transistors manufactured at 22 nm [2], which is the first in the industry to exploit fin based tri-gate devices and combine the benefits of strained silicon and high-k/metal-gate. With a smaller 3D tri-gate transistor, Intel can design even more powerful processors with incredible power efficiency. Critical to the success of the 3D tri-gate technology are the analytical techniques, supporting process development. Transmission electron microscopy (TEM) with its unique atomic resolution and analytical capabilities has become crucial and irreplaceable in technology research and development as well as product manufacturing in the semiconductor industry.

The Intel 22nm transistor continued using epitaxial SiGe for PMOS strain engineering on the new 3D tri-gate architecture [2]. The new tri-gate structure raises more challenges for strain characterization. Optical-based methods can provide a route for macro-scale stress measurements at the die and wafer levels while TEM is the only tool providing nanoscale strain measurement. Traditional TEM strain techniques that work for planar transistors, such as convergent beam electron diffraction and dark-field electron holography, do not apply to tri-gate transistors due to the complicated 3D tri-gate geometry. The only e-beam based technique suitable for the tri-gate transistor is nano-beam electron diffraction (NBED). It has the advantage to well separate the device channel and the overlapping gate materials in diffraction space. Figure 1 shows the 2D strain mapping of a tri-gate transistor along the channel [110] direction and [001] direction. The 2D strain map elucidates the mechanical strain more intuitively and can be used to compare with simulation more accurately, guiding strain engineering development.

The 3D tri-gate architecture also drives TEM characterization into three dimensional analysis. Tomography provides critical structure information which cannot be seen in typical 2D imaging due to the projection effect, especially when the architecture is more and more complicated and overlapped. Providing efficient and accurate 3D tomography results is industry priority in both tomography data acquisition and analysis. We have employed a subpixel registration method for the alignment based on minimization of the least squares difference of image intensities, as well as an iterative approach for the tilt axis adjustment, resulting in a significant reduction in reconstruction artifacts compared to traditional cross-correlation alignment and manual tilt adjustment [3] [4]. Figure 2 shows a scanning transmission electron microcopy (STEM) tomography result from a 22nm PMOS transistor. The missing wedge artifact is minimized with the full tilt needle sample, and the improved alignment as shown in Figure 2b. Figure 2c shows a preliminary Electron Energy Loss Spectroscopy (EELS) result at two different tilt angles from the same sample. Chemical tomography helps when the elements cannot be distinguished in

STEM, and EELS tomography can provide additional bonding information in the fine structure, making it even more powerful.

Transistor technology scaling has been pushing materials characterization into a new era in terms of resolution, sensitivity, multiple dimensions as well as automation for both structural and chemical analysis. Innovative metrologies are always needed to go beyond the requirement and speed of process development in order to maintain the continuity of Moore's Law.

References:
[1] D Hisamoto et al, IEDM (1989) p. 833
[2] C Auth et al, VLSI Technology (2012) p. 131
[3] P Thevenaz et al, IEEE Transaction on Image Processing, volume 7 (1998) p. 27
[4] D Wolf et al, Proceedings of the 15th European Microscopy Congress
[5] ORTEM lab engineers and artists are gratefully acknowledged for the TEM works to support the 22nm tri-gate technology

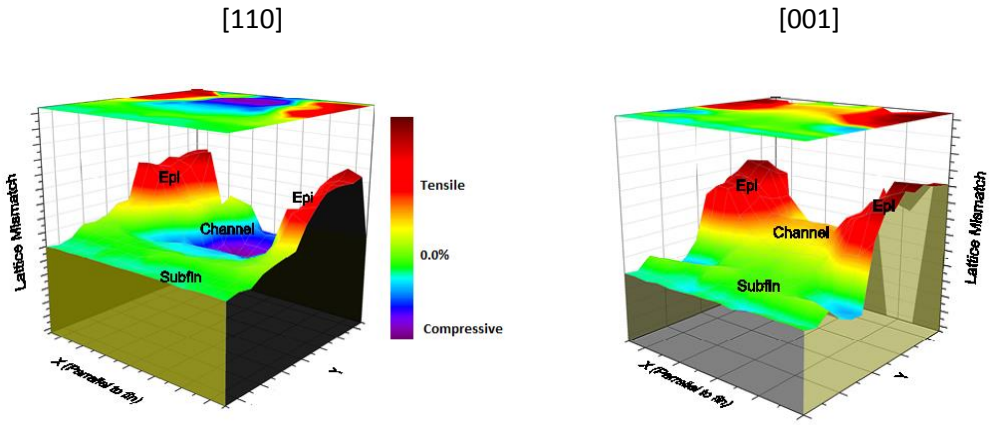


**Figure 1.** NBED strain map of a tri-gate transistor in [110] channel direction and [001] direction.

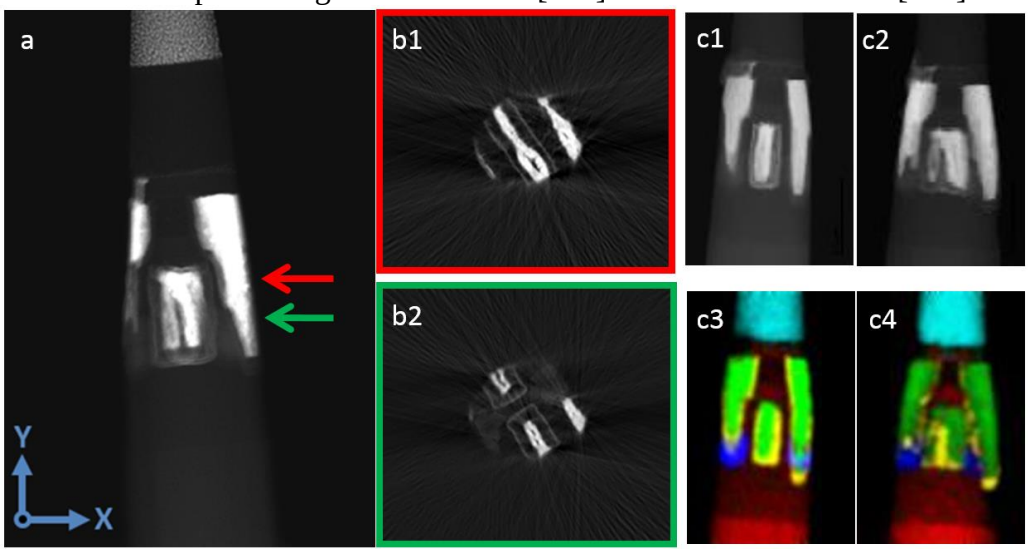


**Figure 2.** STEM tomography of a needle PMOS tri-gate transistor. Slices in (b) are extracted at the locations denoted by arrows in (a). (c) STEM images and EELS maps at two different tilt angles for EELS tomography.

https://doi.org/10.1017/S1431927615012441 Published online by Cambridge University Press