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Sample Preparation for Precise and Quantitative Electron Holography Analysis of Electrostatic Potential in Semiconductor Devices

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Off-axis electron holography has demonstrated its capability for quantitative analysis of electrostatic potential in semiconductor devices by probing phase shifts in electron wave [1]. Currently, most semiconductor device sample preparation for electron holography have been based on focused ion beam (FIB). However, damage related to energetic focused ions has been known as a major problem preventing accurate assessment of the electrostatic potential [2].

In this work, mechanical wedge-polishing was used to prepare electron holography sample of heavily doped ultra-shallow Si junctions for extension regions (or lightly doped drain, LDD)[3] in Si MOSFET devices without any ion milling. Cloth polishing with colloidal silica suspension was used as a final polishing to remove mechanical damage, smooth out the surface, and reach appropriate sample thicknesses (200 ~ 400 nm) for electron holography.

Two different ultra-shallow junctions, n^+/p (nLDD) and p^+/n (pLDD) were fabricated using low energy ion implantation in silicon (100) wafer. After deposition of silicon nitride, silicon oxide (TEOS), and Cr films on samples for protection, wedge-polishing was done using diamond lapping films with grit size in the range of 30 um to 0.1 um. Red Final C cloth and 0.02μm blue colloidal silica suspension with a pH of 9.8 from Allied High Tech Products, Inc. were used for final polishing. Electron holography was performed on a FEI CM 200 FEG equipped with a Lorentz lens and an electron biprism positively biased ~ 120 V to produce holograms.

Figs. 1 (a) and (b) show the SIMS results for the junctions. The metallurgical junction depths were determined to be ~ 25 nm and ~ 12 nm respectively. Figs. 2 (a) and (b) show the representative reconstructed phase images of two junctions. Junction contrast is clearly visible for both junctions as arrowed. Figs. 3 (a) and (b) show the profiles of measured and calculated electrostatic potentials across nLDD and pLDD junctions. A 1-D Poisson solver, developed by Greg Snider [4], was used to calculate the potential profiles across the junctions based on SIMS data with the assumption of 100 % dopant activation. A highest dopant activation limit of $2 \times 10^{20}\text{cm}^{-3}$ [5] during the annealing process was used for simulation. For both nLDD and pLDD junctions, the agreement between calculation and measurement was remarkable except the potential difference (~ 0.87 V) across the pLDD junction was smaller than simulated (~ 1.2 V).

References

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4. The 1D Poisson developed by Greg Snider (online available: http://www.nd.edu/~gsnider/).
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6. Support for this research was provided by the Semiconductor Research Corporation.

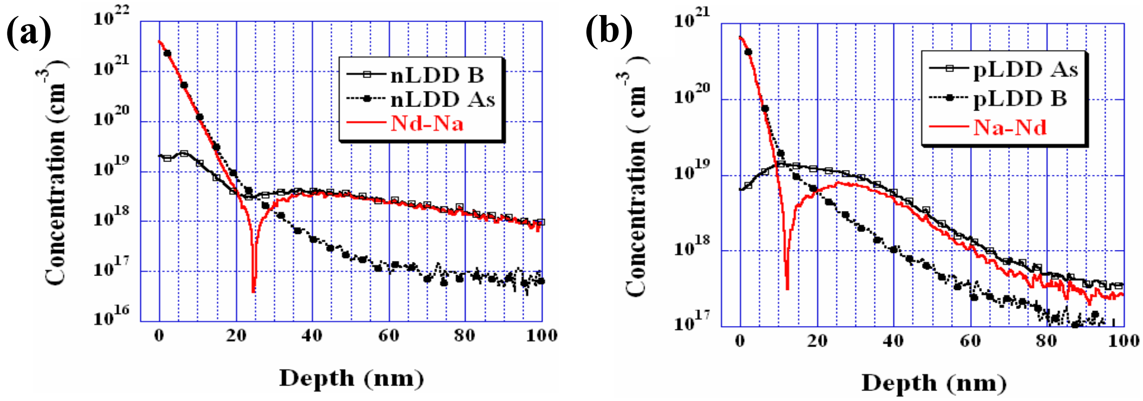

FIG. 1 SIMS results for both (a) nLDD and (b) pLDD junctions. The net dopant concentrations are also shown as an absolute value of the difference between two dopant concentrations.

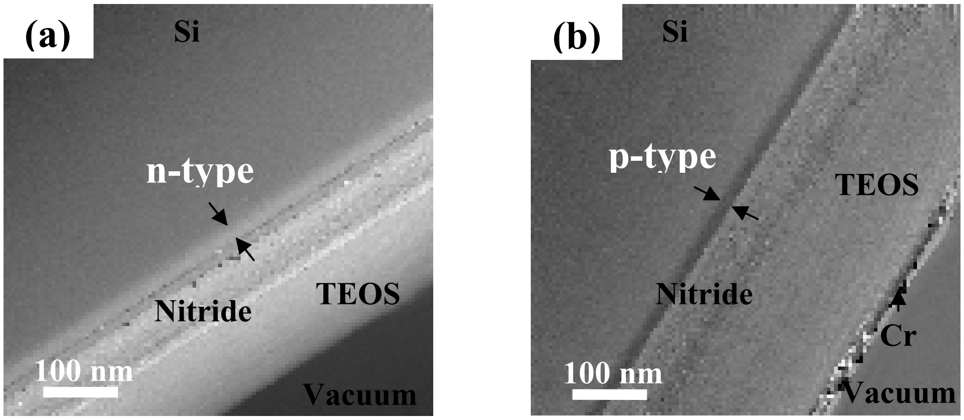

FIG. 2 Reconstructed phase images: (a) nLDD and (b) pLDD samples. The shallow junction contrasts, bright for nLDD and dark for pLDD, are indicated with arrows.

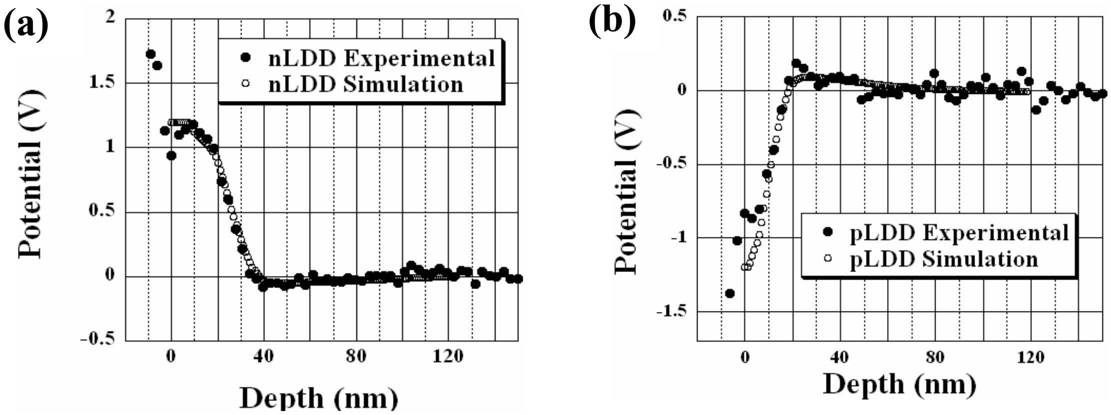

FIG. 3 Potential profiles: (a) across nLDD and (b) pLDD junctions. The reference (0 V) is chosen in the substrate region far from the junction.