



Nano Focus

He droplet method produces narrow distributed nanoparticles as stable catalyst

Conventional synthesis methods for nanoparticles (NPs) suffer from low uniformity, surface contamination, and poor stability, limiting their practical use. A significant step toward overcoming these problems was recently developed by researchers at Stony Brook University, who devised a novel synthesis route based on helium nanodroplet isolation that produces a narrow distribution of clean and stable gold NPs.

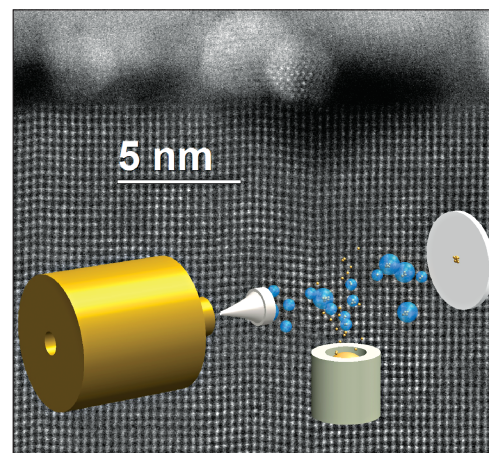
“This is a very powerful method for producing active nanoparticles, which can be extended to other metals [beyond gold]. The helium droplet method produces very clean nanoparticles,” says Alexander Orlov, the leader of the research team in the Department of Materials Science and Chemical Engineering at Stony Brook University, The State University of New York. “By depositing them on any substrates this approach can be applied to produce energy in a clean way, and address environmental issues by oxidizing various atmospheric pollutants,” he adds.

As reported in the July issue of *The Journal of Physical Chemistry Letters* (doi:10.1021/acs.jpcllett.6b01305), Qiyuan Wu and his colleagues created “nanoscale

cryostats” using helium droplets. These droplets capture and condense the vaporized gold atoms, then carry them to the collector. The helium atoms evaporate immediately once they hit a collector, and simultaneously Au atoms form NPs with pristine surfaces.

By varying the nozzle temperature and deposition time, the researchers could tune the size of the resulting NPs, achieving diameters down to <0.75 nm. The method results in a remarkably narrow size distribution, with the variation of the diameter (ΔD) smaller than $0.3D$. This method offers a significant improvement over previously reported synthetic methods for NPs. Exceptional thermal and chemical stability were achieved under CO oxidization reaction conditions, with temperatures up to 475 K.

“This is a significant achievement in synthesizing uniform and clean metal nanoparticles. Without any assistance from organic surface ligands, gold nanoparticles can be produced that exhibit high monodispersity, which would be very useful for heterogeneous catalysis,” says Bo Zhang, an expert in electrocatalysis for clean energy storage at the University of Toronto. To further benefit the catalysis field with the advantages of



Schematic of the growth of Au nanoparticles through the helium droplet method. High-resolution transmission electron microscope image of Au nanoparticles on a substrate. Credit: *The Journal of Physical Chemistry Letters*.

this synthetic method, Bo points out that comparing the CO to CO₂ conversion performance of the new gold nanoparticles with conventional ones at various temperatures would be of great interest.

“The next stage of our research is to fine-tune the shape of nanoparticles, to establish structure–reactivity relations and extend this methodology to other metals,” Orlov says. “We also plan to demonstrate the advantage of this method for accelerating other chemical reactions than carbon monoxide oxidation.”

Xiwen Gong

Nano Focus

Growth of low-temperature Si nanowires suitable for electronic memory devices

Digital information can be stored in magnetic, optical, or semiconductor devices. Although significant breakthroughs have occurred in the development of semiconductor-based memories in the last few decades, further increases in storage density and further miniaturization of memory cells are needed for improved performance. Silicon nanowires (Si NWs), due to their large surface-to-volume ratio and high crystallinity, are a promising candidate for miniaturized memory structures.

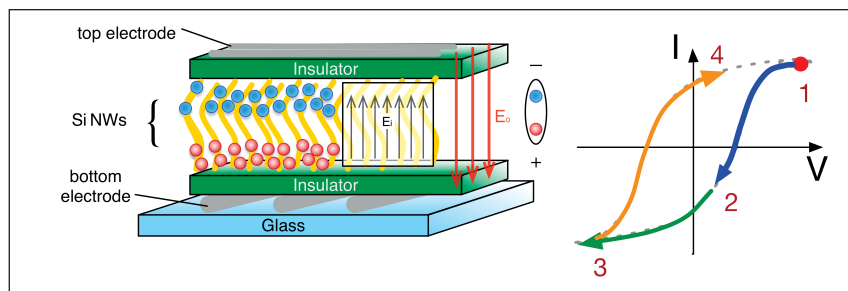


Illustration of schematic two-terminal nonvolatile device (2TNV) with Si nanowires (NWs) as a charge-storage medium in the READ process with applied electrical field E_0 and internal electric field E_i in the opposite direction. The current–voltage hysteresis plot explains the working principle of the 2TNV memory. Credit: *Scientific Reports*.

However, the high growth temperatures and low trapped charge density limits the development of Si NWs-based electronic

devices. A research group has now introduced a new approach to build a two-terminal nonvolatile (2TNV) memory, a device



that utilizes a varying internal electric field between two electrodes to define memory states, using a low temperature Ga-assisted growth and silicon nitride dielectric layer deposition. The device developed by the group exhibits electrical bistability and read-write-erase states under various applied electric potentials.

As reported in a recent issue of *Scientific Reports* (doi:10.1038/srep27506), the research team, led by Shashi Paul in the Emerging Technologies Research Centre at De Montfort University, fabricated Si NW memories with enhanced charging properties to improve memory storage and a low temperature growth method to reduce the device cost.

The Si NWs in the study were grown on a glass slide sandwiched between a silicon nitride dielectric layer and aluminum metal electrodes. Electrical measurements indicate bistable memory states at 0 and 1 under various applied voltages. The research team built a metal-insulator-semiconductor structure to study the charging effects. The results showed large hysteresis due to the enhanced Si NWs charge-storage capacity and long charge retention time.

“The fabrication method [developed] allows controlled growth of silicon nanowires directly on various substrates through the use of an evaporated catalytic layer,” Paul says.

“This extends the use of nanowires for Si-based engineering, science, and the possibilities for a broad range of applications with bottom-up manufacturing.”

“It is exciting that well-aligned silicon nanowires in nonvolatile devices could increase the switching current and improve the electrical bistability,” says Sheng Xu, an assistant professor in the Department of Nanoengineering at the University of California, San Diego, with expertise in the field of nanowire devices. “In addition, these silicon nanowires were fabricated at a low temperature, which holds great implications for scaling up.”

YuHao Liu

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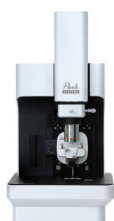
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