

## From Aircraft to Microchips: Science and Technology at the Atomic Scale

D. A. Muller\*

\*School of Applied and Engineering Physics, Cornell University, Ithaca, NY 14853

There is an intimate relationship between the electronic and physical properties of a material. Nowhere is this more pronounced than at interfaces, where the success or failure of a device, be it a turbine blade or a transistor, depends on the bonding changes across a few monolayers[1, 2]. Atomic-resolution electron energy loss spectroscopy (EELS) is now capable of unraveling these bonding details at buried interfaces and clusters, providing both physical and electronic structure information. In some cases the sensitivity and resolution extends to imaging single dopant atoms or vacancies, allowing us to study identify the clusters responsible for electrical deactivation in integrated circuits[3, 4]. In fact, the smallest feature in a modern transistor, the gate dielectric, is already little more than an interfacial layer just over 1 nm thick, and the fundamental physical limits to device scaling are set by the measured electronic structure[1, 5].

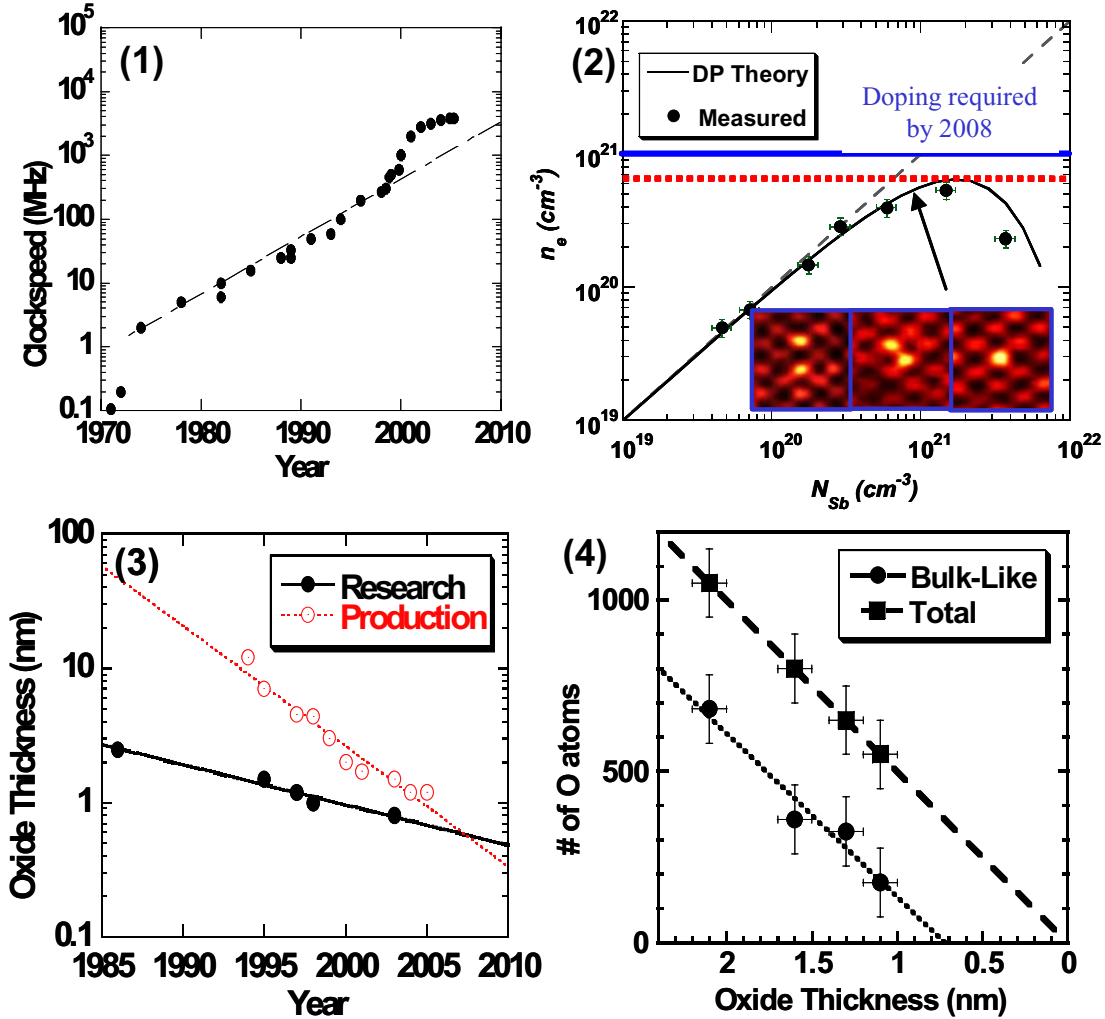
For the first time in thirty five years, the clock speed of the fastest commercial computer chips has not increased (Fig 1). There are three technological challenges that present a “sound barrier” for silicon, in the sense that the cheap, conventional methods of scaling cannot continue and new, potentially expensive solutions must be found. The three challenges are increasing the source and drain dopant concentrations (Fig. 2); shrinking the effective gate oxide thickness (Fig. 3); and shrinking the metal lines that connect the transistors. EELS have had a critical role to play in understanding each of these three areas. We have used atomic-resolution scanning transmission electron microscope with single atom sensitivity to identify the size, structure and distribution of clusters responsible for the saturation of charge carriers and address the question of how many atoms are needed before the gate oxide loses its bulk properties (Fig. 4).

Fig. 2 shows that the dopant concentration cannot be increased without limit, and in fact reaches a maximum at a point below that need for the 2008 generation of devices. Whether this limitation is intrinsic or can be overcome by clever processing is a matter of great concern. From annular dark field STEM images of single Sb dopant atoms buried inside a silicon crystal, we have been able to identify clusters containing only 2 Sb atoms as the defect responsible for the electrical behavior shown in fig. 2[4]. Such clusters are a consequence of a random dopant distribution.

As to the scaling limit for SiO<sub>2</sub> gate oxides, from the analysis of O-K edge EELS fine structure recorded across gate oxides of ever-diminishing thicknesses, we find that the electrical transition region from Si to SiO<sub>2</sub> occurs over a region that is 0.3-0.4 nm wide, even when the structural transition is atomically abrupt. This puts a fundamental limit of 0.7 nm on the oxide thickness in order for the bulk SiO<sub>2</sub> properties to be achieved (fig 4), and provides a challenge for the design of replacement gate dielectrics, many of which contain a few monolayers of SiO<sub>2</sub>. In the search for replacements for the SiO<sub>2</sub> gate oxide, one outstanding problem has been in reducing the fixed charge density in the gate stack, where a flatband or threshold voltage shift of even a few tens of millivolts impacts device performance. The final challenge is in shrinking the metal line width, which requires also shrinking the diffusion barriers surrounding the line to just a few atoms. Atomic-scale chemical reactions in 3D structures can only be detected by EELS, but are critical to the success or failure of the devices.

Until these challenges are addressed through new research, the semiconductor industry risks a commoditization (and similar fate) to the aerospace or automobile industries. [6]

- [1] D. A. Muller, *et al.*, Nature **399**, 758 (1999).
- [2] D. A. Muller, *et al.*, Physical Review Letters **75**, 4744 (1995).
- [3] H.-J. Gossmann, C. S. Rafferty, P. Keys, Mat. Res. Soc. Symp. **610**, B1.2.1 (2000).
- [4] P. M. Voyles, *et al.*, Nature **416**, 826 (2002).
- [5] D. A. Muller, Nature Materials **4**, 645 (2005).
- [6] This work supported by the SRC and Cornell Center for Materials Research, an NSF-MRSEC



**FIG 1.** A “Sound Barrier” for silicon? (a) Clockspeed of Intel microprocessors as a function of time[5]. Is this curve leveling off, or just waiting to catch up?

**FIG 2.** Density of free carriers ( $n_e$ ) as a function of Sb dopant concentration ( $n_{Sb}$ )[4]. The peak carrier concentration (...) still falls below the 2008 semiconductor roadmap requirements[3]. Inset: ADF STEM images of the Sb dopant clusters responsible for the decrease in carrier activation.

**FIG 3.** Effective gate-oxide thickness as a function of time, both for commercially production, and the best reported research results. These results all turn out to be from SiO<sub>2</sub> or nitrided SiO<sub>2</sub> oxides, which outperform their High-k “replacements”.

**FIG 4.** The number of O atoms with bulk-like and interfacial bonding arrangements (as measure by O-K Edge EELS) plotted as a function of gate oxide thickness. There is no more bulk-like silicon dioxide when the gate oxide is less than 0.7 nm thick. Only the interface states remain[1].