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Silicon Chip Teardown to the Atomic Scale – Challenges Facing the Reverse Engineering of Semiconductors

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The first decade of the new millennium has seen both evolution and revolution in silicon processing; many changes in silicon chip processing, and the introduction of new materials in the latest product generations has presented huge challenges to the industry. The relentless progress of Moore's law has seen five generational shrinks in the last ten years, from the 130-nm node through the 90, 65, and 45-nm nodes to the 32-nm node chips launched at the beginning of this year. The dimensions of essential chip features are now measurable on the atomic scale – gate dielectrics are 3-4 molecules thick, and a 25-nm gate is <70 Si atoms long!

This progress has been achieved by a number of significant changes in:

- Lithography – the transition from 248 nm→193 nm→ 193 nm immersion
- Materials – Al→Cu, low-k dielectrics, high-k dielectrics, metal gate, resist chemistry
- Application of strain techniques – stress liners, embedded SiGe, shallow trench isolation
- Sensitivity to random effects/defects, e.g. dopant fluctuation, line edge roughness.

These challenges have been the drivers for the evolution of analytical techniques in the semiconductor industry. Ten years ago we could see the essential structure of a chip with SEM techniques, with the occasional use of TEM to examine crystalline structure; now features sizes are so small that HRTEM is obligatory and we have to consider the use of other tools such as atom probe tomography.

Chipworks, as a supplier of competitive intelligence to the semiconductor and electronics industries, monitors the evolution of chip technologies as they come into commercial production. Chipworks has obtained parts from the leading edge manufacturers, and performed structural and compositional analyses to examine the features and manufacturing processes of the devices.

This paper illustrates some of the different techniques used to examine the structures and composition of semiconductor devices seen in the last few years from some of the leading companies in the sector, ranging from the 90-nm node to the latest 32-nm Intel microprocessor. Representative images are shown on page 2 of this abstract.

Reference:

[1] L. Klibanov et al., *"Doping Profile Measurements in a 65-nm Commercial Product using Atom Probe Tomography"*, ISTFA 2008

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TEM Images of PMOS Transistor from Intel 32-nm CPU

TEM Plan-View Section of Samsung 48-nm DRAM

3D Reconstruction of Elemental Data from 65-nm Transistor Gate Analyzed by Atom Probe Tomography [1]

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