# Aberration Corrected Microscopy and Moore's Law: Capabilities Aiding Progress for the Next Decade

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In 1965, Gordon Moore wrote a landmark paper that with only five data points, predicted the number of components in an integrated circuit would double every 18 months[1]. In 1975, the rate was scaled back to doubling every two years, but in the past 30 years, that scaling has continued without interruption. Since chips cannot grow in size indefinitely, a corollary to Moore's Law has been that the size of features in each chip must shrink accordingly so that more components can be accommodated on each chip. As the size of these features is reduced, switching speeds improve, resulting in devices with performance improvements that have scaled upwards in accordance with Moore's Law. Indeed, the insatiable desire for higher performance has been a major driver for the pursuit of Moore's Law. In 2004, products manufactured using a nominal 90nm feature size became commercially available. Since device scaling is expected to continue without interruption, ten years from now products manufactured using a nominal 22nm feature size should become commercially available[2],[3]. Up until the turn of the century, scaling of well known materials was all that was needed to continue Moore's Law: silicon oxide gates were made thinner, poly silicon lines were made narrower, patterned aluminum lines and the insulators between them were made thinner, planarization became mandatory, and more layers of circuitry were added. However, the past few years have seen the introduction of new materials, with more being developed, because simply shrinking traditional gates, metal wiring, and dielectrics could not continue to provide the performance improvements that are expected with each new generation of devices.

The first big change in materials has already taken place, and that has been in the metal wiring. Patterned aluminum insulated by subsequent deposition of silicon oxide, has been replaced by damascene copper embedded in a 'low-$K$' insulator. In coming years, the 'copper-low-$K$' technology will be tuned for higher performance, with modifications of the metal for reliability and modifications of the insulator for performance. Unfortunately, all of the insulator materials on the horizon show degraded mechanical properties, which pose problems for both manufacturing and making TEM specimens.

The second big change has been implementation of strained transistors, through more than one mechanism, but retaining the basic CMOS FET design. Changes on the horizon include a transition from silicon oxide gate dielectrics to 'high-$K$' dielectrics such as hafnium, zirconium or aluminum oxides, changes in gate material from poly silicon to 'non-silicon' materials, changes in the basic design of planar MOS transistors to either silicon on insulator and/or three dimensional transistors such as tri-gate[2], fin-FET, vertical transistors[4], nano-tubes, nano-wires, or some other design yet to be seen. These material changes on top of continued shrinking of structures will require that atomic scale microscopy and microanalysis be carried out as a daily routine, with quick data through-put on thousands of specimens per year, a task best suited to an aberration-corrected TEM.

Another consequence of the continual device shrink is that commercial products today incorporate complex fabricated non-planar structures having dimensions comparable to or smaller than the

thickness of a traditional TEM specimen.  As a result, conventional cross-sectioning and imaging can yield unsatisfactory results that are difficult to interpret due to geometrical blurring. Electron tomography shows great promise for contributing to a solution to this conundrum.  In another paper[5] we present results on 3D reconstructions from tilt series, both in bright field and HAADF from samples of vias. We found that a wider gap pole piece Super Twin Tecnai F20 using HAADF with its unconstrained single tilt produced significantly better results than a narrow gap pole piece Ultra Twin CM30 with its constrained tilt even when two orthogonal tilt axes were combined. Achieving higher resolution without the experimental constraints of an ultra-narrow-gap pole piece is a requirement that can be fulfilled best by an aberration-corrected microscope.

References

[1] G. E. Moore, Electronics, Vol. 38 No. 8, April 19, 1965
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[3] http://public.itrs.net/
[4] http://www.bell-labs.com/project/feature/archives/verticaltransistor/
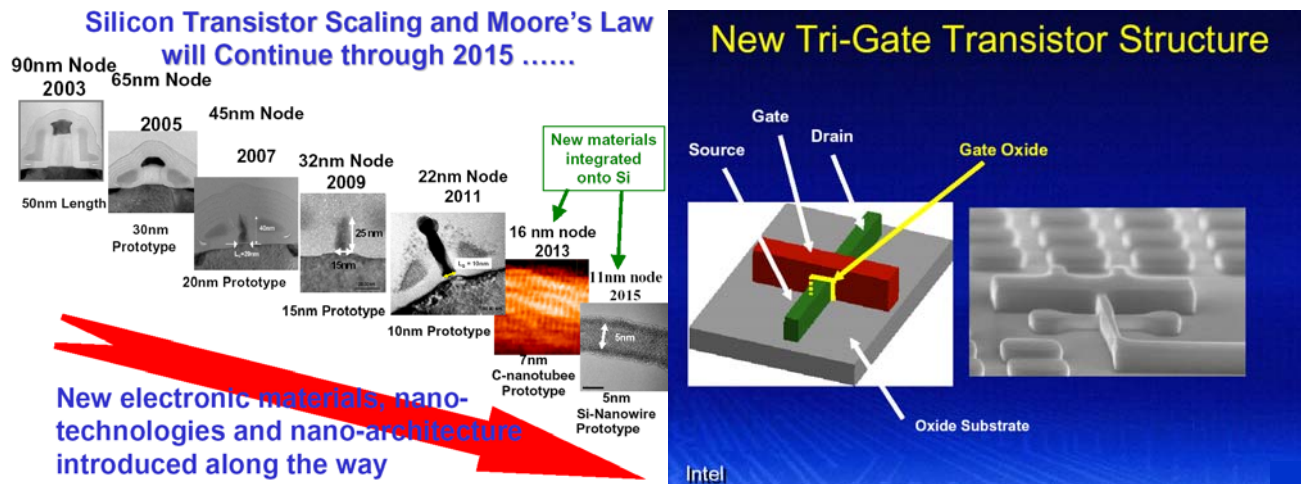[5] Q. Yang, J. Mardinly, Microscopy and Microanalysis, Vol.8, August 2005

Fig. 1. a) Transistor roadmap, showing one possible scenario for the evolution of transistor design during the next decade, and b) More detail of one possible three-dimensional transistor in which the gate surrounds the channel.
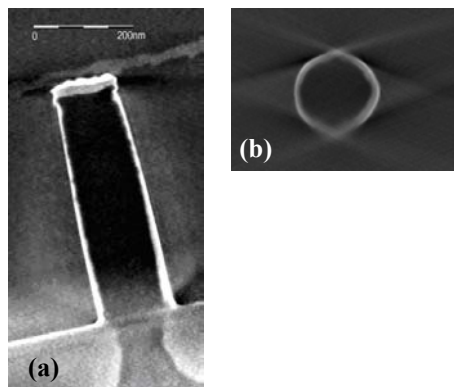


Fig. 2. Slices from tomogram reconstructed using 155 STEM-HAADF images tilted around one axis at 1° intervals.  (a) Y-Z slice parallel to the TEM sample surface. (b) Slice perpendicular to the sample surface and the long axis of the via.