

In-situ TEM Characterization of Ultra-robust Memristors Based on Fully Layered Two-dimensional Materials

Songhua Cai¹, Miao Wang², Xiaoqing Pan^{1,3}, J. Joshua Yang⁴, Feng Miao², Peng Wang¹

¹ National Laboratory of Solid State Microstructures, College of Engineering and Applied Sciences and Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing, China.

² School of Physics, Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing, China.

³ Department of Chemical Engineering and Materials Science and Department of Physics and Astronomy, University of California, Irvine, CA, USA.

⁴ Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA, USA.

Memristor is a promising candidate for storage and neuromorphic electronics in the future [1] because of advantages such as device scalability, multi-state storage, high switching speed and endurance, as well as CMOS compatibility [2]. While the reliability of memristors in extreme environments such as high temperature and bending substrates has not been much studied yet, we designed and fabricated an ultra-robust memristor consists of a Van der Waals (vdW) heterostructure laminated with graphene/MoS_{2-x}O_x/graphene, all fully layered 2D materials. Our test suggests a total life up to 10⁷ cycles and ultra-high thermal stability that can work properly even temperature up to 340°C [3]. These results show that vdW heterostructures made up through stacked 2D layered materials can integrate each component's unique properties then fit actual requirements in detection and production.

To investigate the temperature stability of the heterostructural device, we carried out a TEM in-situ heating test to same MoS_{2-x}O_x used in our devices. MoS_{2-x}O_x nanosheets were prepared by ultrasonic exfoliation then dropped onto a DENSsolution in-situ heating chip. Before in-situ experiment, sample was heated to 160°C in atmosphere and kept 90 mins for thermal oxidation. In-situ heating results prove that layered MoS_{2-x}O_x can still retain undamaged up to 800°C, exhibits excellent thermal stability. From HRTEM images and FFT results, the lattice constant of MoS_{2-x}O_x was measured to be 3.16Å at room temperature, which matches former reported values [4]. At 800°C, the actual lattice constant slightly increased to 3.19Å, indicates a tiny lattice thermal expansion and expansion ratio is about 1%.

Furthermore, we carried out *in situ* scanning transmission electron microscopy (STEM) investigations to investigate the working mechanism of GMG memristor. *In-situ* device sample was made by FEI helios 600i dual-beam FIB system and fabricated to our home made in-situ electrical testing chip. HAADF and STEM-EDS analyses were used to reveal structure change and mass migration during switching process. The STEM and HRTEM images were obtained on a FEI Titan Cubed G2 60-300 aberration corrected S/TEM. The operation voltage of 60 kV was used to reduce electron beam damage to graphene and MoS_{2-x}O_x. EDS analyses were carried out using Bruker SuperEDX four-detector system. By switching the device to ON/OFF states inside the S/TEM, we were able to observe the structural changing area of the conduction channel in MoS_{2-x}O_x layer in real-time and attributed the switching mechanism to the migration of oxygen ions. The numbers of Mo, S and O were measured and normalized as atom percentage. MoS_{2-x}O_x layer in pristine state shows a normal atom distribution with Mo : (S+O) ≈ 1 : 2. Then at ON state a reduction of S and O atoms was observed in conduction channel region, where Mo : (S+O) is about 1 : 1.2. At OFF state, an increase of O atoms was observed in conduction channel region, led to ratio of Mo

: (S+O) back to near 1 : 2. As a result, the changing of oxygen vacancy intensity caused two different resistance states.

References:

- [1] L Chua, IEEE Trans. Circuit Theory **18** (1971), p. 507.
 [2] J Yang, D Strukov and D Stewart, Nat. Nanotechnol. **8** (2013), p. 13.
 [3] M Wang, *et al*, Nature Electronic (2018), <https://doi.org/10.1038/s41928-018-0021-4>.
 [4] S Helveg, *et al*, Phys. Rev. Lett. **84** (2000), p. 5.

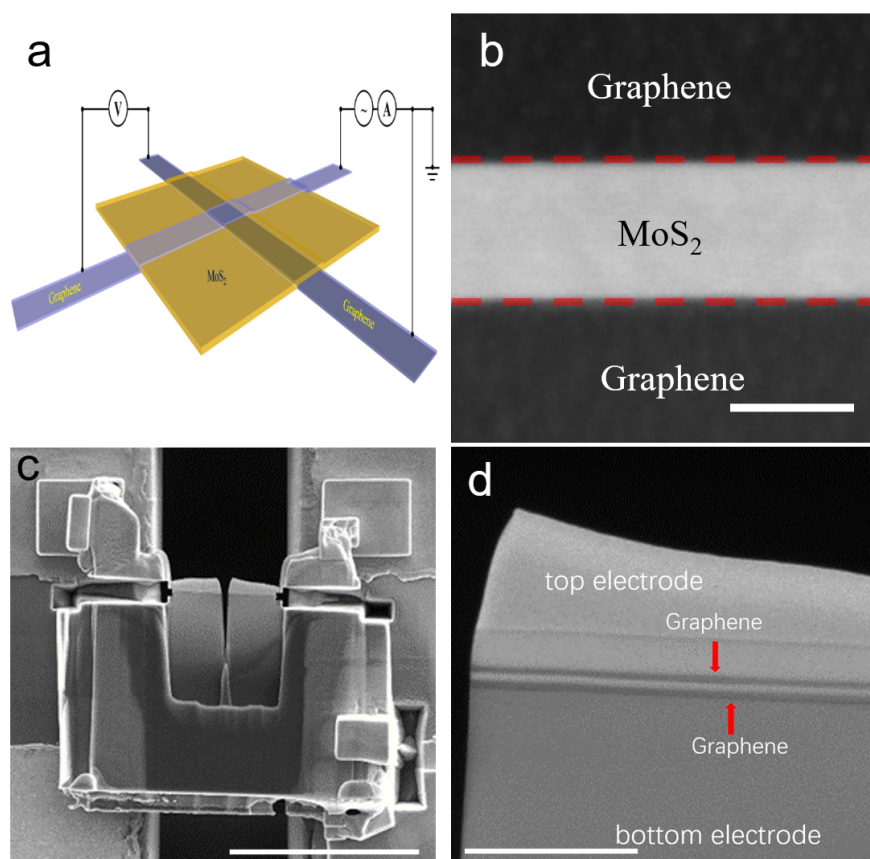


Figure 1. (a) schematic drawing of the GMG devices. (b) Cross-section HAADF image of a pristine GMG device. Scale bar: 20 nm. (c) in-situ GMG device sample welded on home-made in-situ electrical testing chip by dual-beam FIB system. Scale bar: 10 μ m. (d) high magnification SEM image of in-situ cross section sample, shows a sandwich structure. Scale bar: 1 μ m.