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Frequency analysis of load modulation networks for asymmetric Doherty power amplifiers in GaN

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Research Paper

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Abstract

This paper investigates the frequency response of load modulation networks for asymmetric Doherty power amplifiers (ADPA) with an output back-off power level larger than 6 dB and a power ratio of peak to main amplifier $(N-1)$ larger than 1. The influence of the main path impedance transformer (IT) on the Doherty impedances at main and peak path as well as on the ADPA's efficiency is analyzed. Scaling of the main IT's characteristic impedance via ξ indicates a maximum broadband matching for an input voltage V_{in} of $\xi \cdot V_{\text{in,max}}$. By weighting the frequency- and ξ-dependent efficiency curves using a probability density function (PDF), an optimum is obtained for $\xi = 1/N$. To verify the theory, three ADPAs with different ξ-scaled ITs are designed, measured, and compared. For the design at 3.6 GHz, a gallium nitride (GaN) transistor is used. By means of the intrinsic node matching technique, matching at the current source plane is obtained. In laboratory measurements, the ADPA with $\xi = 1/N$ achieves a power-added efficiency (PAE) of 63% at 42 dBm output power and a PDF-weighted average PAE of 38.8% within 400 MHz bandwidth for 8 dB peak-to-average power ratio. Comparison with similar state-of-the-art ADPAs in GaN technology shows highest PAE and operation power gain G_{P} for center frequencies larger than 3.0 GHz.

Introduction

The design of next generation wireless communication systems revolves around two main aspects: increasing data rates and power efficiency. In order to meet these growing demands, modulation schemes with instantaneous bandwidths of more than 200 MHz and dynamic ranges with peak-to-average-ratios (PAPR) of up to 12 dB are utilized to ensure gigabit-per-second transmission in the sub 6 Ghz frequency bands.

In a radio frequency transmitter, the major part of power consumption is caused by the power amplifier (PA). Hence, an energy-efficient system has to tap into its maximum power saving potential. Since an analog amplifier reaches maximum drain efficiency (DE) merely at maximum output power, several topologies, such as envelope tracking, out-phasing, or Doherty PA (DPA) [1], have been proposed to increase efficiency in the output back-off (OBO) region. The DPA topology will be the focal point of this work with an in-depth examination of its broadband behavior.

This paper builds upon previous works [2, 3] which identify the impedance transformer (IT) as bandwidth bottleneck by analyzing the frequency response of the Doherty load modulation network. Furthermore, the ITs' impact on the Doherty impedances at the main path $\underline{Z}_{\text{M}}$ and peak path $\underline{Z}_{\text{P}}$ is demonstrated in [4]. A comprehensive overview of investigated techniques for bandwidth extension (e.g. modification of the output network, parasitic compensation, dual-input, and transformer-less load modulation) is provided in [5]. However, these investigations are always based on the symmetric DPA topology with OBO = 6 dB, neglecting signals with a PAPR above 6 dB.

In this work, previous frequency analyses are extended by including the asymmetric DPA (ADPA) with an OBO larger than 6 dB. Further, the effects of the main path IT on the DE, $\underline{Z}_{\text{M}}$, and $\underline{Z}_{\text{P}}$ for broadband performance are examined.

A scaling factor ξ, which is used to vary the characteristic impedance of the main path IT, is introduced in the theory section "Analysis of the asymmetric Doherty modulation network with a scaled impedance transformer". Depending on ξ, a maximum broadband matching of the main amplifier at a specific input level can be achieved. By weighting the frequency- and ξ-dependent efficiency curves using Rayleigh distributed probability density function (PDF), an optimum is found at $\xi = 1/N$. This theory is proven by the design of three amplifiers with different values of ξ. The design procedure at 3.6 GHz is described in section "Design process of the proposed Doherty power amplifier". For the design, a commercial gallium nitride (GaN) transistor model, which enables an intrinsic node matching technique, is used. The results obtained from laboratory measurements are presented in section

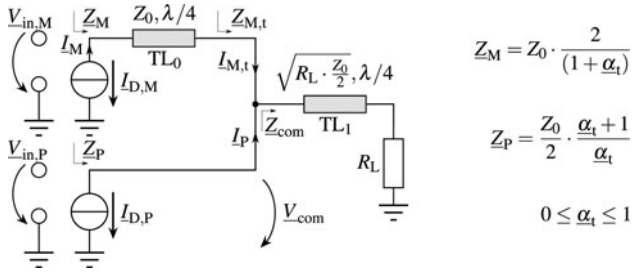

Fig. 1. Schematic of a classical Doherty load modulation network.

"Experimental results" and finally compared with the state-of-the-art in section "Conclusion". Leading up to the theoretical analyses in section "Analysis of the asymmetric Doherty modulation network with a scaled impedance transformer", the introduction section contains a brief review of the classical Doherty architecture.

Underlined parameters in this work, such as $\underline{\alpha}_t$ or $\underline{Z}_M$, indicate a complex value.

Classical Doherty load modulation network

A classical symmetric Doherty modulation network is shown in Fig. 1. At the common node of the main and peak path an impedance $\underline{Z}_{com} = Z_0/2$ is provided. Moreover, Z_0 determines the impedances $\underline{Z}_M$ and $\underline{Z}_P$. Those impedances further depend on the modulation index after impedance transformation $\underline{\alpha}_t$, which is the ratio of the peak path current $\underline{I}_P$ to the transformed main path current $\underline{I}_{M,t}$. Since the peak amplifier must provide the same output current as the main amplifier at maximum input voltage $\underline{V}_{in,max}$ and no current below the back-off threshold at $\underline{V}_{in,max}/2$, $\underline{\alpha}_t$ is described by

$$\underline{\alpha}_t = \begin{cases} 0 & 0 \le V_{in} < V_{in,max}/2 \\ \frac{\underline{I}_P}{\underline{I}_{M,t}} & V_{in,max}/2 \le V_{in} \le V_{in,max} \end{cases}. \tag{1}$$

Thus, a voltage amplitude at the peak amplifier input $\underline{V}_{in,P}$ occurs for $V_{in} > V_{in,max}/2$. This is realized by class C biasing of the peak amplifier.

Impedances provided by the classical Doherty modulation network

$\underline{Z}_M$ and $\underline{Z}_P$ are now determined at the output node of the voltage-controlled current sources. The transformed impedance $\underline{Z}_{M,t}$ after the IT of the main path TL$_0$ is calculated with

$$\underline{Z}_{M,t} = \frac{\underline{V}_{com}}{\underline{I}_{M,t}} = \frac{Z_0}{2} \cdot \frac{\underline{I}_{M,t} + \underline{I}_P}{\underline{I}_{M,t}} \tag{2}$$

and transformed by TL$_0$ to

$$\underline{Z}_M = \frac{Z_0^2}{\underline{Z}_{M,t}} = \frac{2 \cdot Z_0}{(1 + \frac{\underline{I}_P}{\underline{I}_{M,t}})} = \frac{2 \cdot Z_0}{(1 + \underline{\alpha}_t)}. \tag{3}$$

The Doherty impedance of the peak path $\underline{Z}_P$ is determined with

$$\underline{Z}_P = \frac{\underline{V}_{com}}{\underline{I}_P} = \frac{Z_0}{2} \cdot \frac{\underline{I}_{M,t} + \underline{I}_P}{\underline{I}_P} = \frac{Z_0}{2} \cdot \frac{\underline{\alpha}_t + 1}{\underline{\alpha}_t}. \tag{4}$$

To transform the load impedance R_L to $\underline{Z}_{com}$, a second λ/4 IT TL$_1$ with the characteristic impedance

$$Z_1 = \sqrt{R_L \cdot \frac{Z_0}{2}} \tag{5}$$

is used.

Analysis of the asymmetric Doherty modulation network with a scaled impedance transformer

As described in a previous work [6], it is advantageous to modify the classical (symmetric) Doherty modulation network toward an asymmetric Doherty modulation network. This enables a more efficient performance for signals with a PAPR > 6 dB. The output power ratio between peak amplifier $P_{out,P}$ and main amplifier $P_{out,M}$ can be described by

$$\frac{P_{out,P}}{P_{out,M}} = 10^{OBO/20} = N - 1. \tag{6}$$

For an asymmetric topology with OBO larger than 6 dB, $(N-1)$ is larger than 1. The load modulation in dependence of N was thoroughly investigated in [6], however a frequency analyses was not carried out and shall be part of the proposed work.

Determination of the impedance Z_0

The common node impedance $\underline{Z}_{com}$ in an asymmetric Doherty modulation network is Z_0/N. As depicted in Fig. 2 it is transformed from the load R_L by TL$_1$ with a characteristic impedance Z_1 of

$$Z_1 = \sqrt{R_L \cdot \frac{Z_0}{N}}. \tag{7}$$

For a classical DPA, the frequency response of $\underline{Z}_{com}$ is analyzed in [5]. In case of a more general asymmetric topology, this expands to

$$\underline{Z}_{com} = \frac{Z_0}{N} \cdot \frac{\frac{1}{m} + j \cdot \tan\left(\frac{\pi}{2}\frac{f}{f_0}\right)}{m + j \cdot \tan\left(\frac{\pi}{2}\frac{f}{f_0}\right)} \tag{8}$$

with

$$m = \sqrt{\frac{Z_0}{N \cdot R_L}}. \tag{9}$$

For $m = 1$, the frequency dependent part of (8) is canceled. This is achieved at

$$Z_0 = R_L \cdot N. \tag{10}$$

By inserting (10) into (8) one obtains

$$\underline{Z}_{com} = R_L, \tag{11}$$

thus no bandwidth limiting IT is necessary and TL$_1$ can be omitted. If for design reasons a Z_0 different from (10) is necessary, a

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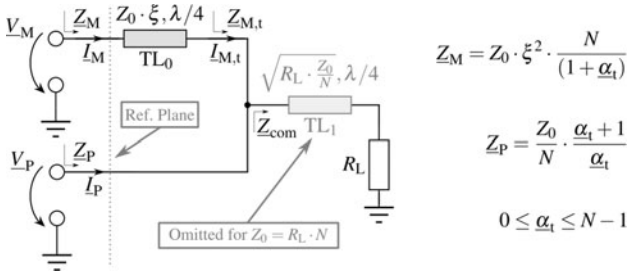

Fig. 2. Schematic of the proposed Doherty load modulation network with a $Z_0 \cdot \xi$ TL_0 impedance transformer.

broadband post matching network should be used. Several works, such as [4, 7], provide solutions for this task.

Main path impedance provided by a Doherty modulation network with scaled impedance transformer

The characteristic impedance of TL_0 can be chosen freely, even if Z_0 is already defined by (10). Hence, ξ is now introduced as scaling variable. For the proposed Doherty load modulation network in Fig. 2, the impedance analysis is carried out at the output nodes of the ideal current sources as reference plane. According to (3), the extended calculation for $\underline{Z}_M$ follows:

$$\underline{Z}_M = \frac{(Z_0 \cdot \xi)^2}{\underline{Z}_{M,t}} = Z_0 \cdot \xi^2 \cdot \frac{N}{(1+\underline{\alpha}_t)}. \tag{12}$$

The ratio of the peak path to the main path current needs to satisfy the equation

$$\frac{|\underline{I}_P|}{|\underline{I}_M|} = \xi \cdot (N-1) \tag{13}$$

to ensure the correct ratio of $\underline{I}_{M,t}$ and $\underline{I}_P$ at the common node for $V_{in} = V_{in,max}$.

Frequency analysis of the load modulation in the main path

The previous calculations are only valid at the design frequency f_0. However, the topology related λ/4 IT TL_0 lowers the ADPA's bandwidth independently of the main or peak amplifier bandwidth. $\underline{Z}_M$ and $\underline{Z}_P$ are real-valued at f_0. Below and above this frequency, imaginary parts occur and subsequently the real part changes. This causes mismatch and thus a reduction in the efficiency of the amplifier. Moreover, a phase shift between the main and peak path current appears at the common node of the main and peak path, which is not compensated by the λ/4 IT at the peak amplifier input. The summation of $\underline{I}_{M,t}$ and $\underline{I}_P$ becomes complex-valued, thus the ratio $\underline{\alpha}_t$, previously defined in (1), also depends on the frequency.

To analyze the Doherty load modulation network and its impedances $\underline{Z}_M$ and $\underline{Z}_P$ in the frequency domain, the reference plane in Fig. 2 is used as input of a two-port network. The two-port equation in ABCD-parameters yields

$$\begin{bmatrix} \underline{V}_M \\ \underline{I}_M \end{bmatrix} = \begin{bmatrix} \underline{A}_M & \underline{B}_M \\ \underline{C}_M & \underline{D}_M \end{bmatrix} \cdot \begin{bmatrix} \underline{V}_{M,t} \\ \underline{I}_{M,t} \end{bmatrix}. \tag{14}$$

The transmission parameters for the lossless transmission line TL_0 with $Z_0 \cdot \xi$ as its characteristic impedance are

$$\begin{bmatrix} \underline{A}_M & \underline{B}_M \\ \underline{C}_M & \underline{D}_M \end{bmatrix} = \begin{bmatrix} \cos\left(\frac{\pi}{2}\frac{f}{f_0}\right) & j \cdot Z_0 \cdot \xi \sin\left(\frac{\pi}{2}\frac{f}{f_0}\right) \\ \frac{j}{Z_0 \cdot \xi}\sin\left(\frac{\pi}{2}\frac{f}{f_0}\right) & \cos\left(\frac{\pi}{2}\frac{f}{f_0}\right) \end{bmatrix}. \tag{15}$$

The voltage at the common node $\underline{V}_{com}$ can be expressed by

$$\underline{V}_{com} = \underline{V}_{M,t} = \underline{V}_P = (\underline{I}_{M,t} + \underline{I}_P) \cdot \underline{Z}_{com}. \tag{16}$$

Inserting (16) into (14), the voltage $\underline{V}_M$ and current $\underline{I}_M$ at the main path input are defined by

$$\underline{V}_M = \underline{A}_M \cdot (\underline{I}_{M,t} + \underline{I}_P) \cdot \underline{Z}_{com} + \underline{B}_M \cdot \underline{I}_{M,t} \tag{17}$$

$$\underline{I}_M = \underline{C}_M \cdot (\underline{I}_{M,t} + \underline{I}_P) \cdot \underline{Z}_{com} + \underline{D}_M \cdot \underline{I}_{M,t}. \tag{18}$$

Rearranging (18) to $\underline{I}_{M,t}$ and inserting it into (17) yields $\underline{V}_M$ in dependency of the two input currents:

$$\begin{aligned} \underline{V}_M = \underline{A}_M \cdot \left(\frac{\underline{I}_M - \underline{C}_M \cdot \underline{I}_P \cdot \underline{Z}_{com}}{\underline{C}_M \cdot \underline{Z}_{com} + \underline{D}_M} + \underline{I}_P\right) \cdot \underline{Z}_{com} \\ + \underline{B}_M \cdot \left(\frac{\underline{I}_M - \underline{C}M \cdot \underline{I}_P \cdot \underline{Z}_{com}}{\underline{C}_M \cdot \underline{Z}_{com} + \underline{D}_M}\right). \end{aligned} \tag{19}$$

Dividing (19) by $\underline{I}_M$ one obtains $\underline{Z}_M$. According to (13), the ratio of the current amplitudes $|\underline{I}_M|$ and $|\underline{I}_P|$ can now be expressed as

$$\frac{|\underline{I}_P|}{|\underline{I}_M|} = \begin{cases} 0 & 0 \le V_{in} < \frac{V_{in,max}}{N} \\ \xi \cdot \left(N - \frac{V_{in,max}}{V_{in}}\right) & \frac{V_{in,max}}{N} \le V_{in} \le V_{in,max}. \end{cases} \tag{20}$$

For a complex-valued peak-to-main current ratio before transformation $\underline{\alpha}$, a phase shift of π/2 at f_0 between $\underline{I}_P$ and $\underline{I}_M$ has to be considered, which is provided by the λ/4 IT at the peak amplifier input:

$$\underline{\alpha} = \frac{\underline{I}_P}{\underline{I}_M} = |\underline{\alpha}| \cdot e^{-j \cdot (\pi/2)(f/f_0)}. \tag{21}$$

Thus, the Doherty impedance of the main path $\underline{Z}_M$ without saturation can be described by

$$\begin{aligned} \underline{Z}_M = \underline{A}_M \cdot \left(\frac{1 - \underline{C}_M \cdot \underline{\alpha} \cdot \underline{Z}_{com}}{\underline{C}_M \cdot \underline{Z}_{com} + \underline{D}_M} + \underline{\alpha}\right) \cdot \underline{Z}_{com} \\ + \underline{B}_M \cdot \left(\frac{1 - \underline{C}_M \cdot \underline{\alpha} \cdot \underline{Z}_{com}}{\underline{C}_M \cdot \underline{Z}_{com} + \underline{D}_M}\right). \end{aligned} \tag{22}$$

To take the saturation of the main amplifier current source into account, a maximum drain-source voltage $V_{DS,M,max}$ is defined based on $I_{D,M,max}$ and $\underline{Z}_M(\underline{\alpha}_t = 0)$ at f_0:

$$V_{DS,M,max} = I_{D,M,max} \cdot Z_0 \cdot \xi^2. \tag{23}$$

The behavior considering saturation is conditioned with

$$\underline{V}_M = \begin{cases} \underline{V}_M & |V_M| \le V_{DS,M,max} \\ V_{DS,M,max} & |V_M| > V_{DS,M,max}. \end{cases} \tag{24}$$

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In case of $|V_M| > V_{DS,M,max}$, the ideal voltage-controlled current source turns into an ideal voltage-controlled voltage source. To describe $\underline{Z}_{M,sat}$ for this case, (19) is used with $\underline{V}_M$ equal to $V_{DS,M,max}$ to express the saturation current as

$$\underline{I}_{M,sat} = \frac{(V_{DS,M,max} - \underline{A}_M) \cdot (\underline{C}_M \cdot \underline{Z}_{com} + \underline{D}_M)}{\underline{A}_M \cdot \underline{Z}_{com} + \underline{B}_M} + \frac{\underline{Z}_{com} \cdot \underline{I}_P \cdot (\underline{A}_M \cdot \underline{C}_M \cdot \underline{Z}_{com} + \underline{B}_M \cdot \underline{C}_M)}{\underline{A}_M \cdot \underline{Z}_{com} + \underline{B}_M}. \quad (25)$$

Finally, the Doherty impedance for the main path with saturation results in

$$\underline{Z}_{M,sat} = \begin{cases} \underline{Z}_M & |V_M| \le V_{DS,M,max} \\ \frac{V_{DS,M,max}}{\underline{I}_{M,sat}} & |V_M| > V_{DS,M,max} \end{cases}. \quad (26)$$

Fig. 3 illustrates the contours of $\underline{Z}_{M,sat}$ for three different values of ξ by sweeping the input voltage from back-off to maximum level, as well as the frequency from $0.5 \cdot f_0$ to $1.5 \cdot f_0$. The crossing of the real axis occurs at f_0. On the left side, the saturation causes the straightening of the curves due to the limited magnitude of $\underline{Z}_{M,sat}$. For the input voltage

$$V_{in,\xi} = \xi \cdot V_{in,max}, \quad (27)$$

$\underline{Z}_{M,sat}$ is solely real-valued over the frequency and equal to the characteristic impedance of TL_0. Thus, a maximum broadband matching is reached at this point, which can be defined via ξ. In Fig. 3, these points are highlighted respectively.

Frequency analysis of the load modulation in the peak path

For the peak path, similar considerations can be made. Taking (16) and (18) into account, the peak amplifier Doherty impedance $\underline{Z}_P$ can be derived. Here, the saturation effect for the peak amplifier can be neglected, since the chosen characteristic impedance for TL_1 of $R_L \cdot N$ leads to a coherent addition of the currents $\underline{I}_{M,t}$ and $\underline{I}_P$. Thus, the highest impedance or voltage magnitude always occurs at f_0. The saturation of the main amplifier however affects the peak path, which is why a distinction between $\underline{I}_M$ and $\underline{I}_{M,sat}$ has to be considered for the calculation $\underline{Z}_P$ given by

$$\underline{Z}_P = \frac{\underline{V}_P}{\underline{I}_P} = \left(\frac{\frac{\underline{I}_{M/M,sat}}{\underline{I}_P} - C_M \cdot \underline{Z}_{com}}{C_M \cdot \underline{Z}_{com} + D_M} + 1 \right) \cdot \underline{Z}_{com}. \quad (28)$$

In Fig. 4, the impedance curves for $\underline{Z}_P$ are shown for the same conditions as for Fig. 3. The effect of saturation of the main amplifier is less pronounced for $\underline{Z}_P$. For input voltages below $V_{in,max}/N$, $\underline{Z}_P$ approaches infinity. With increasing V_{in}, either the real ($\xi = 1$) or the imaginary ($\xi = 1/N$) part of $\underline{Z}_P$ increases. Here, the maximum broadband matching at $V_{in,\xi}$ becomes also evident.

The performance for signals with a larger bandwidth depends mostly on the broadband matching properties. However, the ξ-scaled IT is only matched at $V_{in,\xi}$. Simultaneous matching at back-off and peak level is not achieved. To find the best tradeoff, the impact on the drain efficiency of the ADPA will be examined in the following segment.

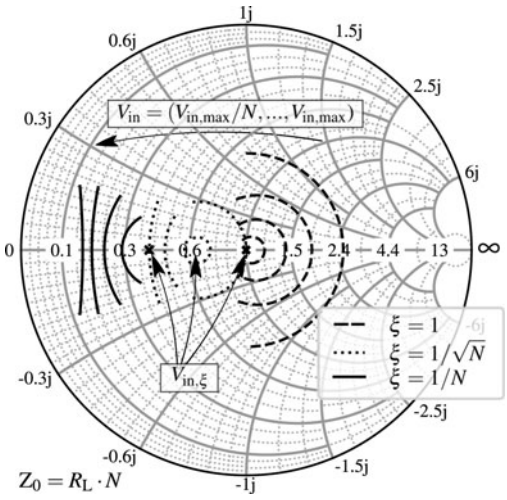

Fig. 3. Curves of the Doherty impedances at the reference plane of the main path $\underline{Z}_{M,sat}$ versus frequencies from $0.5 \cdot f_0$ to $1.5 \cdot f_0$ for different values ξ and $N = 2.5$ while sweeping the input voltage V_{in} with input voltages $V_{in,\xi}$ for a maximum broadband matching highlighted.

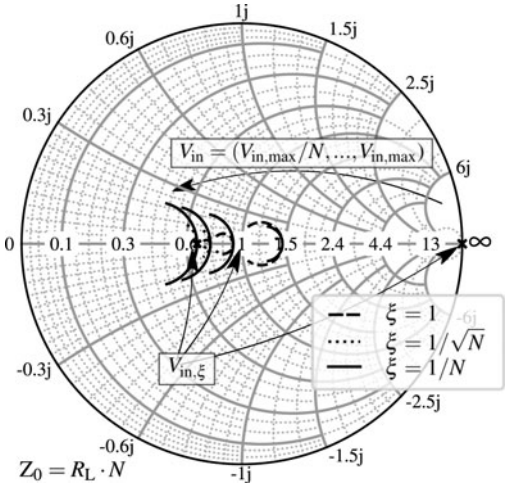

Fig. 4. Curves of the Doherty impedances at the reference plane of the peak path $\underline{Z}_P$ versus frequencies from $0.5 \cdot f_0$ to $1.5 \cdot f_0$ for different values ξ and $N = 2.5$ while sweeping the input voltage V_{in}.

Frequency analysis of the drain efficiency

Given the preliminary discussion, an ADPA's DE can be considered. With amplifiers biased in class B, the ratio of RF output power to DC power consumption for Fig. 2 follows:

$$DE = \frac{\pi}{4} \cdot \frac{|\underline{I}_M|^2 \cdot \mathrm{Re}(\underline{Z}_{M,sat}) + |\underline{I}_P|^2 \cdot \mathrm{Re}(\underline{Z}_P)}{|\underline{I}_M| \cdot V_{DS,M,max} + |\underline{I}_P| \cdot V_{DS,P,max}}. \quad (29)$$

The DE curve with its two efficiency peaks at back-off and maximum output power level is now derived for different frequencies. For broadband signals, this consideration is necessary to reach a high overall efficiency. As illustrated in Fig. 5, the efficiency trajectories beside f_0 are affected by the frequency-dependent Doherty impedances $\underline{Z}_{M,sat}$ and $\underline{Z}_P$. For $\xi = 1/N$ and $\xi = 1$, they only reach one efficiency peak at $V_{in,\xi}$. With $\xi = 1/\sqrt{N}$, $V_{in,\xi}$ is between back-off and maximum input level, so these curves have a local

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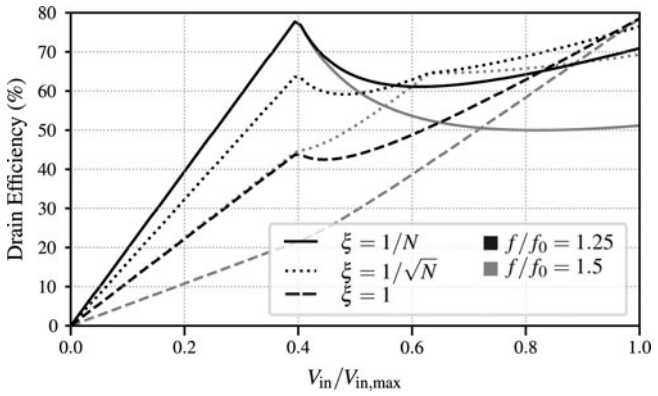

Fig. 5. Drain efficiency DE versus normalized input voltage V_{in} beside f_0 for $N = 2.5$ and different values of ξ.

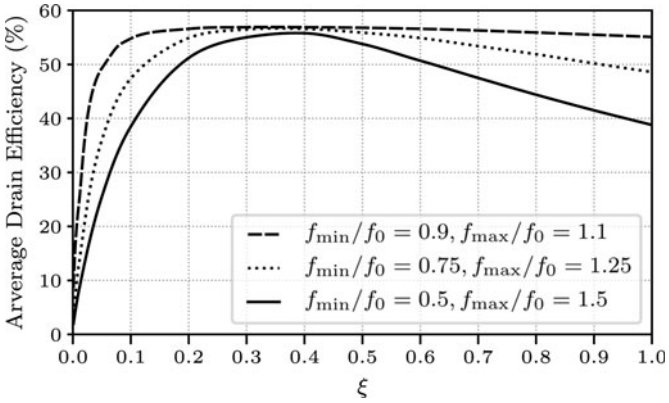

Fig. 6. Averaged drain efficiency versus ξ for Rayleigh-distributed signals of different relative bandwidths with $N = 2.5$, $Z_0 = R_L \cdot N$.

maxima in between. For a classical Doherty load modulation network where $\xi = 1$ and $N = 2.5$, the back-off DE at $f/f_0 = 1.25$ is just 42% and further drops to 21% at $f/f_0 = 1.5$. Otherwise, a high efficiency is reached at maximum input level due to maximum broadband matching.

Drain efficiency depending on probability density function

In order to estimate the broadband efficiency, a PDF-weighted input signal is used. The overall PDF-weighted efficiency $DE_{PDF,B}$ within a bandwidth

$$B = f_{max} - f_{min} \tag{30}$$

can be defined as

$$DE_{PDF,B} = \frac{1}{B} \cdot \int_0^1 \int_{f_{min}}^{f_{max}} DE(V_{in}, f) \cdot PDF(V_{in}) df \, dV_{in}. \tag{31}$$

To analyze the previous load modulation networks, a Rayleigh distribution defined by

$$PDF_{Ray}(V_{in}) = \frac{V_{in}}{\sigma^2} \cdot e^{-V_{in}/2\sigma^2} \tag{32}$$

is utilized as an example.

With $\sigma = 1/N \cdot \sqrt{2/\pi}$, the expected value arises at OBO which meets the desired PAPR. As stated in (31), the PDF is considered only for the input voltage, while the distribution is uniform over frequency. Fig. 6 compares $DE_{PDF,B}$ for the three different bandwidths, while ξ is swept. For the used PDF with a PAPR of 8 dB, the highest efficiency is reached at $\xi = 0.4$, which corresponds to $\xi = 1/N$. The optimum becomes all the more obvious with increasing bandwidth. Moreover, to ensure maximum efficiency, $V_{in,\xi}$ should meet the expected value. This principle was also found to be true for signals with an uniform PDF. The estimation of the system efficiency should be based on the PDF of the signal to be transmitted and not exclusively on DE curves. This approach should already be considered in the design process.

Design process of the proposed Doherty power amplifier

To prove the theory of section "Analysis of the asymmetric Doherty modulation network with a scaled impedance transformer", an ADPA with three representative values for $\xi = (1/N, 1/\sqrt{N}, 0.8)$ is designed. The selected values of ξ result in different characteristic impedances for TL_0. Thus, further practical effects of the Doherty IT shall be investigated. In this section, the amplifier design procedure, its matching technique, and the implemented input and output matching networks (OMNs) are covered.

The schematic of the proposed circuit is depicted in Fig. 7. A GaN high electron mobility transistor (HEMT) *CG2H40010F* by *Wolfspeed/Cree* is used on a *Rogers4350* 254 µm substrate. Using SMD components instead of λ/4 lines for biasing networks, DC-blocking and input splitter minimizes the required board area yielding a more compact design. According to the fifth generation mobile communications standard (5G), the targeted operation frequency band reaches from 3.4 GHz to 3.8 GHz. The ADPA will be optimized for signals with a PAPR of 8 dB driving a load $R_L = 50\ \Omega$ with its output-related 1 dB compression point at $P_{out,1dB} = 42$ dBm and the first efficiency peak at $P_{out,OBO} = 34$ dBm, respectively. According to (10), Z_0 is set to 125 Ω to avoid additional bandwidth limitations by TL_1. For an OBO of 8 dB, N becomes 2.5 according to (6). Hence, the characteristic impedance of the λ/4 line TL_0 is obtained as follows: 50 Ω for $\xi = 1/N$, 79.1 Ω for $\xi = 1/\sqrt{N}$, and 100 Ω for $\xi = 0.8$.

Optimum load determination with intrinsic node method

Beside the common load-pull method to determine the optimum load for a PA, the current and voltage waveforms at the current source plane of the active device can be used [8]. Since the theoretical considerations of the modulation network are carried out at the current source plane, the parasitics of the package, landing pads, and bias network have to be taken into account for the matching procedure. Fig. 8 illustrates the impedances at different reference planes as well as the two-port blocks transforming the impedances between these planes. Fortunately, the used transistor model allows to simulate current and voltage waveforms of the intrinsic drain node. According to the desired output power and bias conditions, a real-valued load line $R_{OPT,int}$ is applied to its output characteristics.

To determine the optimal intrinsic load for the main amplifier $R_{OPT,M,int}$ and for the peak amplifier $R_{OPT,P,int}$, the transistors are biased in a deep class AB with $V_{Bias,M/P} = -2.9$ V. According to the advantages described in [6], an asymmetric drain biasing of $V_{DD,M} = 18$ V and $V_{DD,P} = 28$ V is used. The main PA has to

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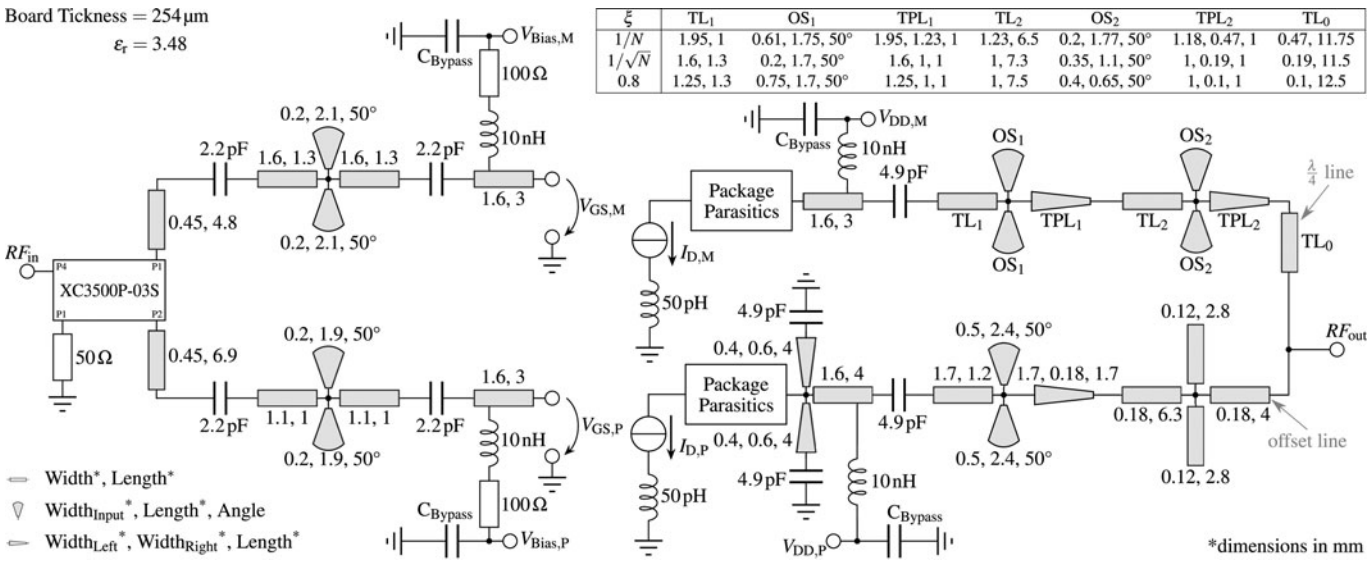

ξ	TL_1	OS_1	TPL_1	TL_2	OS_2	TPL_2	TL_0
$1/N$	1.95, 1	0.61, 1.75, 50°	1.95, 1.23, 1	1.23, 6.5	0.2, 1.77, 50°	1.18, 0.47, 1	0.47, 11.75
$1/\sqrt{N}$	1.6, 1.3	0.2, 1.7, 50°	1.6, 1, 1	1, 7.3	0.35, 1.1, 50°	1, 0.19, 1	0.19, 11.5
0.8	1.25, 1.3	0.75, 1.7, 50°	1.25, 1, 1	1, 7.5	0.4, 0.65, 50°	1, 0.1, 1	0.1, 12.5

Fig. 7. Schematic and design details of the proposed ADPA.

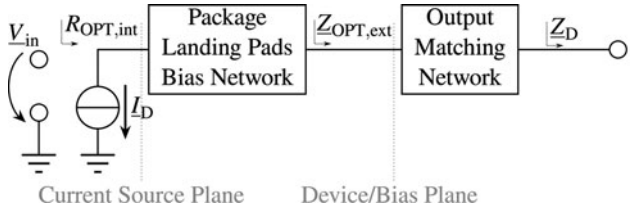

Fig. 8. General schematic of the packaged active device with parasitic and matching network block.

reach an output power of $P_{out,M,OBO} = 34$ dBm at OBO ($\underline{\alpha} = 0$) and $P_{out,M,PEP} = 38$ dBm at peak envelope power (PEP, $\underline{\alpha} = N - 1$), while the peak PA is turned off at OBO and delivers a $P_{out,P,PEP} = 40$ dBm at PEP. Thus, one obtains

$$R_{OPT,M,int}(\underline{\alpha} = 0) = 49.5\,\Omega \tag{33}$$

at OBO and

$$R_{OPT,M,int}(\underline{\alpha} = N - 1) = 32.4\,\Omega \tag{34}$$

at PEP for the specific device and bias conditions. The peak amplifier $R_{OPT,P,int}$ yields

$$R_{OPT,P,int}(\underline{\alpha} = N - 1) = 33.7\,\Omega \tag{35}$$

at PEP.

Based on these values, the impedance at the device/bias plane is varied to identify the optimum external load $\underline{Z}_{OPT,ext}$, which transforms to $R_{OPT,int}$ at the intrinsic node. The corresponding impedance characteristics for the main amplifier between OBO and PEP and for the peak amplifier at PEP are shown in Fig. 9. $R_{OPT,int,M}$ and $R_{OPT,int,P}$ are independent of frequency and located on the real axis. Depending on the frequency, they are transformed from the current source plane to the device/bias plane to $\underline{Z}_{OPT,ext,M}$ and $\underline{Z}_{OPT,ext,P}$, respectively.

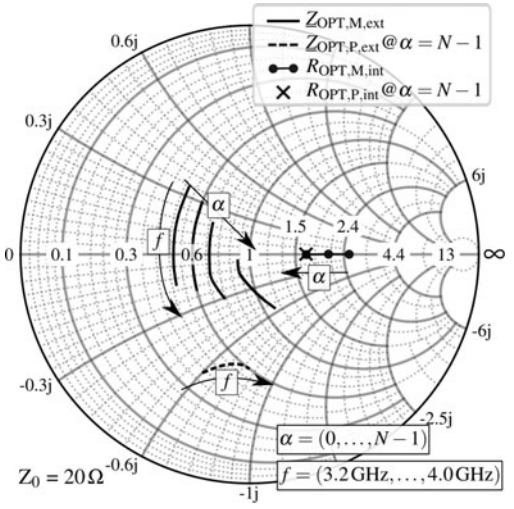

Fig. 9. Optimum intrinsic load $R_{OPT,int}$ and external impedance $\underline{Z}_{OPT,ext}$ derived from intrinsic node method for main amplifier with $\underline{\alpha} = (0, \ldots, N-1)$ and peak amplifier with $\underline{\alpha} = N - 1$ over the frequency range from 3.2 GHz to 4.0 GHz.

Output matching network design

The OMN of the main amplifier has to transform the Doherty impedance $\underline{Z}_M$ to the previously determined impedances $\underline{Z}_{OPT,M,ext}$. According to (12), this OMN depends on the modulation index $\underline{\alpha}$ and the scaling factor ξ. To simplify the design procedure and keep the complexity of the OMN moderate, $\underline{Z}_{OPT,M,ext}$ at the center frequency of 3.6 GHz is used with $\underline{\alpha} = 0$ and $\underline{\alpha} = N - 1$, respectively. This impedance has to be transformed from $\underline{Z}_M(\underline{\alpha}, \xi)$ as specified in Table 1.

The OMN is realized as double-cascaded transmission line open-stub design, which avoids the use of lossy SMD components. An optimization algorithm is used to determine the optimal dimensions meeting the upper defined transforming conditions for each value of ξ.

The design of the peak amplifier's OMN, which transforms its Doherty impedance $\underline{Z}_P$ to $\underline{Z}_{OPT,P,ext}$, is less complex. The fixed

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Table 1. Values for the main amplifier's Doherty impedance $\underline{Z}_M$ with $N = 2.5$, $Z_0 = R_L \cdot N$, and $f = 3.6$ GHz

$\underline{Z}_M(\underline{\alpha}, \xi)$	$\xi = 1/N$	$\xi = 1/\sqrt{N}$	$\xi = 0.8$	$\underline{Z}_{OPT,M,ext}$
$\underline{\alpha} = 0$	50 Ω	79.1 Ω	100 Ω	→ (10 + j · 2) Ω
$\underline{\alpha} = N - 1$	20 Ω	31.6 Ω	40 Ω	→ (20 − j · 7) Ω

matching is independent of $\underline{\alpha}$ and ξ. For the operation below the OBO, the peak amplifier is turned off and should behave as an open circuit at the common node connection. However, this is prevented by the capacitive off-state output impedance of a HEMT. To counteract this, RF shorted-stubs at the landing pad of the drain terminal and the offset line technique [9] were used to push the off-state-impedance of the peak amplifier toward the infinity region. These techniques are a further limiting aspect of an efficient broadband DPA operation due to their frequency dependence. However, the comparability for different values of ξ is maintained due to an identical peak amplifier design. The optimal external impedance at 3.6 GHz is determined with $\underline{Z}_{OPT,P,ext} = (11 - j \cdot 13)\ \Omega$. Using (4), this impedance has to be transformed from $\underline{Z}_P = 83.3\ \Omega$.

Input matching network design

For the main amplifier's input matching, a tradeoff between high efficiency and gain in the targeted bandwidth was found at an input impedance of $(8 - j \cdot 35)\ \Omega$ with its gate bias set to $V_{Bias,M} = -2.9$ V. Due to the class C biasing of the peak amplifier with $V_{Bias,P} = -4.5$ V and a different optimum output impedance, the optimum input impedance is $(8 - j \cdot 25)\ \Omega$. As shown in Fig. 7, both input matching networks are realized in similar element combinations with minor differences in their dimensions. The 100 Ω resistors in the gate biasing paths ensure unconditional stability.

The λ/4 input delay line in the peak path and the power divider at the input are combined by using the 3 dB hybrid coupler *XC3500P-03S* by *Anaren*. It enables a constant 90° phase shift within a bandwidth from 3.3 GHz to 3.85 GHz leading to a more robust performance versus frequency. Moreover, this SMD component is much smaller than an equivalent microstrip line solution.

Large signal simulation for main amplifier

Fig. 10 depicts the simulated large signal performance of the designed main amplifiers including their input and output networks. To demonstrate the influence of the load modulation network, it is necessary that the different main amplifiers achieve as equal a performance as possible. Within the targeted frequency range of 3.4 GHz to 3.8 GHz, the operating power gain G_P and power-added efficiency (PAE) of $\xi = 1/N$ and $\xi = \sqrt{1/N}$ are almost identical. The main amplifier with $\xi = 0.8$ has about 0.5 dB less gain at 3.8 GHz but achieves a higher PAE performance at OBO and PEP. Outside the operating frequency, the deviations increase slightly.

Further design aspects

To simulate the design more accurately, a parasitic inductor of 50 pH is added to the simulation test bench at the source node

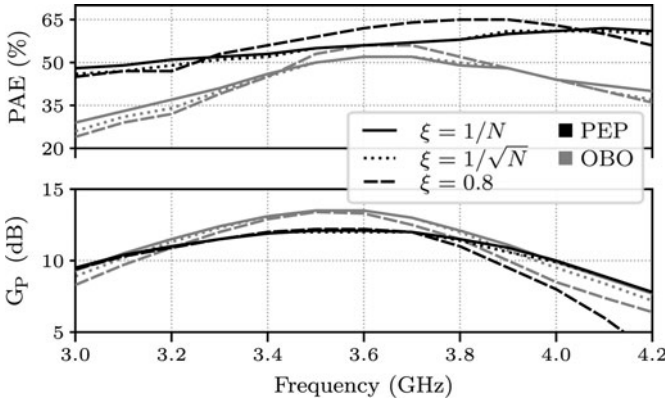

Fig. 10. Simulated PAE and G_P versus frequency at OBO ($P_{out,M,OBO} = 34$ dBm) and PEP ($P_{out,M,PEP} = 38$ dBm) for main amplifiers with $\xi = 1/N$, $1/\sqrt{N}$ and 0.8.

of the transistor. It lowers the gain performance and should be kept as low as possible. To support this, a copper plate with a cavity was manufactured, where the source plate of the transistor is plugged in. In addition, mechanical stability and cooling is provided.

For the input matching network and DC blocking, high-Q multilayer ceramic capacitors *GJM0335C1E2R2WB0* (input matching and DC block) and *GJM0335C2A4R9BB01* (output DC block) by *Murata* were used. A small 0201 (0603 metric) package size with low inductive parasitics is required to ensure the operation below self resonance frequency.

Experimental results

For each value of ξ an ADPA was set-up and measured. Fig. 11 shows the test board for $\xi = 1/\sqrt{N}$. As central measurement instrument, the *R&S® ZVA67* network analyzer was calibrated and used for small signal as well as large signal (continuous wave) measurements. To measure the ADPA performance for modulated signals with a certain PAPR, the *R&S® SMBV100A* signal generator was used.

For the targeted large signal power levels of about 42 dBm with an expected power gain of about 10 dB for a single stage ADPA, an additional driver and attenuator were necessary. The *Mini Circuits ZVE-8G* was used as pre-driver. This driver has a saturated output power of 33 dBm. Hence, to achieve the desired output power of 42 dBm within this measurement setup, an operation power gain of more than 9 dB would be required.

Due to device-related threshold voltage variations between −3.6 V and −2.4 V, the bias voltage $V_{Bias,M}$ of the main amplifier has to be carefully adjusted to obtain an operating current $I_{D,M} =$ 40 mA [10]. For the peak amplifier, the bias voltage $V_{Bias,P}$ needs to be determined by large signal measurements. This is realized by applying an input power resulting in an output power slightly above the OBO. At this point, a noticeable rise of the peak amplifier's drain current $I_{D,P}$ becomes apparent indicating its activation. By this method the bias voltages $V_{Bias,P}$ are adjusted between −4.3 V and −4.2 V.

Small signal measurements

The scattering parameters of the three ADPAs were measured and compared with the simulated behavior. Since the peak amplifier is biased in class C mode, it is not active for the small signal

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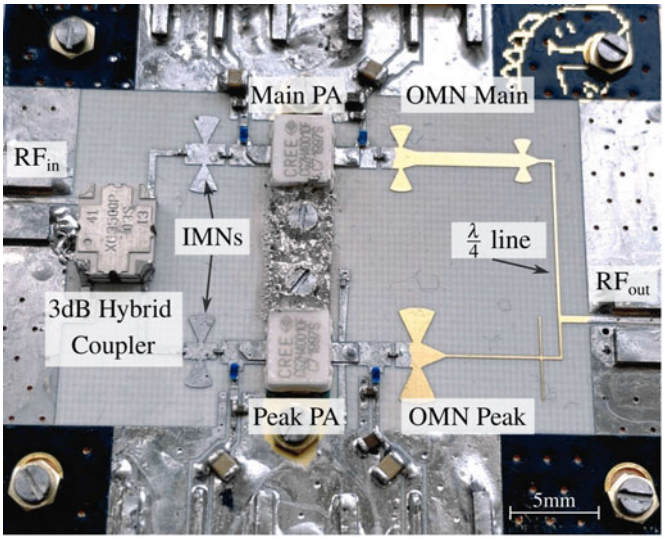

Fig. 11. Photograph of manufactured ADPA for $\xi = 1/\sqrt{N}$, board dimensions: 47.5 mm × 39 mm.

measurement. Thus, this measurement mostly reflects the main amplifier performance. Fig. 12 illustrates the forward gain $S_{21,\mathrm{dB}}$ and the input reflection coefficient $S_{11,\mathrm{dB}}$ for the simulated and measured ADPAs. For $\xi = 1/N$, the measured small signal bandwidth and gain have the highest value. It reaches a maximum gain of 12.3 dB at 3.6 GHz and a 3 dB bandwidth of 700 MHz. The simulated deviation of $S_{21,\mathrm{dB}}$ between $\xi = 1/N$ and $\xi = 0.8$ is about 0.5 dB. For the measurement, it increases to 1.5 dB. One possible reason is better matching of $\xi = 1/N$ at low input levels, which is also advantageous for process variations. Furthermore, a larger deviation can be observed between 4 GHz and 5 GHz where $S_{11,\mathrm{dB}}$ is higher than −5 dB. The resonance might be caused by the cavity in the copper plate, but it is outside the frequency range of interest.

Large signal measurements

To measure the output power, the PAE and the large signal behavior of the ADPAs, single tone signals were applied. The input power was swept up to 33 dBm for frequencies ranging from 3.0 GHz to 4.2 GHz. The achieved PAE and operating power gain G_P performances versus P_out at 3.4 GHz, 3.6 GHz, and 3.8 GHz are shown in Fig. 13. The measured results coincide well with the simulation. In terms of G_P as well as PAE, the amplifier with $\xi = 1/N$ achieves the best performance. Although advantageous in theory, $\xi = 1/\sqrt{N}$ and $\xi = 0.8$ do not exhibit the expected broadband matching for output powers above the OBO.

Since the major investigation was done for broadband performance, the measured PAE and G_P are plotted over frequency in Fig. 14. Here, three output power levels (34 dBm, 38 dBm, 42 dBm) were selected. For $P_\mathrm{out} = 34$ dBm, representing the OBO as well as the $V_{\mathrm{in},\xi}$ of $\xi = 1/N$, the respective ADPA has the highest PAE over the entire bandwidth. Between 3.4 GHz and 3.8 GHz, a PAE of around 45% was measured for $\xi = 1/N$. At 3.2 GHz the PAE difference between $\xi = 1/N$ and $\xi = 0.8$ was around 10%. For P_out of 38 dBm, which corresponds to $V_{\mathrm{in},\xi}$ for $\xi = 1/\sqrt{N}$, the ADPA with $\xi = 1/N$ still has the highest PAE. Especially in the frequency range from 3.1 GHz to 3.7 GHz, a

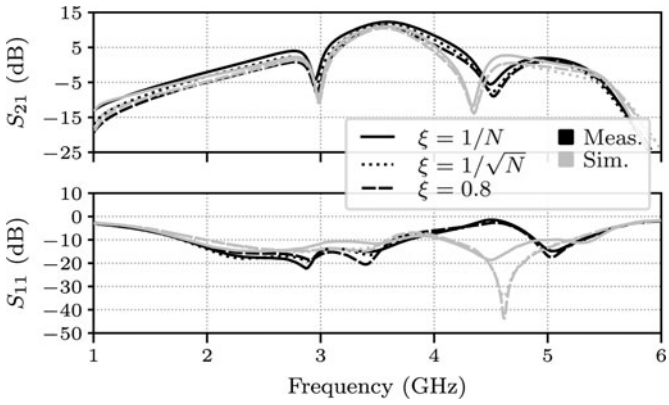

Fig. 12. Measured ($\xi = (1/N, 1/\sqrt{N}, 0.8)$) and simulated ($\xi = 1/N$) forward gain $S_{21,\mathrm{dB}}$ and input reflection coefficient $S_{11,\mathrm{dB}}$ versus frequency of the designed ADPAs.

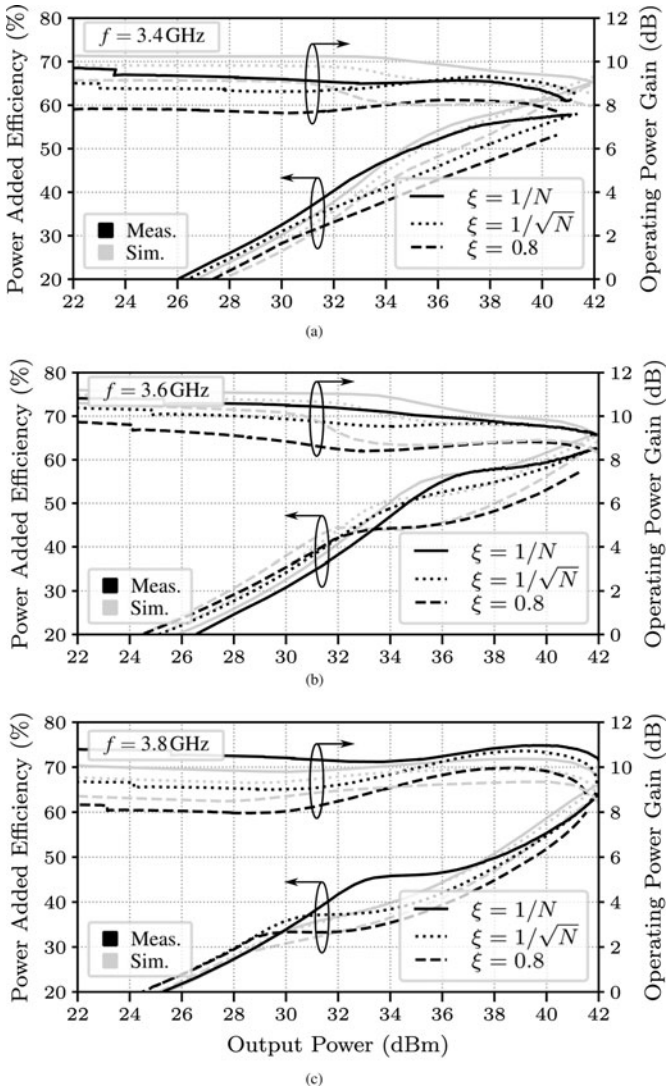

Fig. 13. Measured and simulated power-added efficiency and operating power gain over output power P_out at 3.4 GHz, 3.6 GHz, and 3.8 GHz for ADPAs with $\xi = 1/N$, $1/\sqrt{N}$, and 0.8.

constant difference of about 9% compared to $\xi = 0.8$ can be observed. For the PEP output power of 42 dBm, the PAE curves of $\xi = 1/N$ and $\xi = 1/\sqrt{N}$ are very similar and range from 57%

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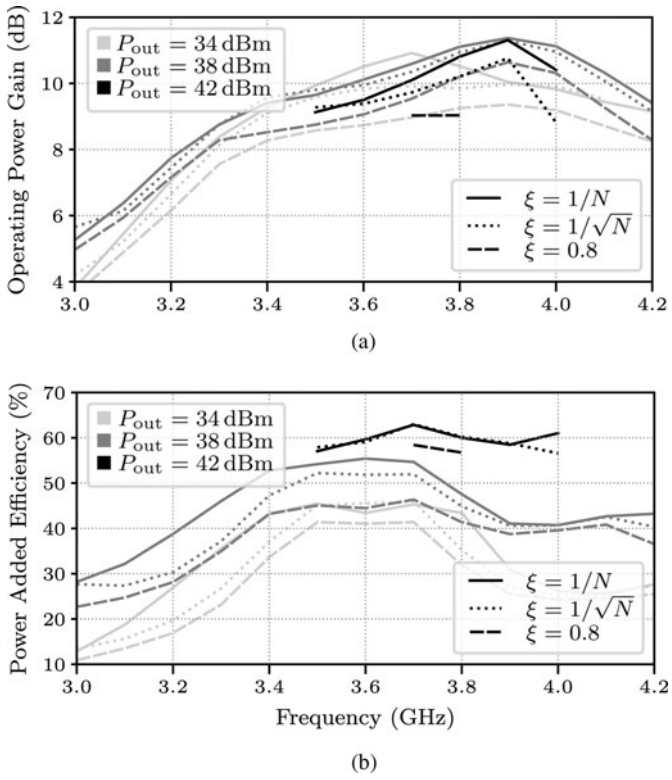

Fig. 14. Measured operating power gain G_P and power-added efficiency of different output power levels P_{out} over frequency for the ADPAs with $\xi = 1/N$, $1/\sqrt{N}$, and 0.8.

to 63% in the frequency band between 3.5 GHz and 4.0 GHz. The ADPA with $\xi = 0.8$ achieves $P_{out} = 42$ dBm only between 3.7 GHz and 3.8 GHz. Within this 200 MHz bandwidth, it even has 5% less PAE of 58%. For frequencies that are not within this range, its G_P drops below 9 dB. Hence, an output power of 42 dBm could not be measured here.

Table 2 compares the measured large signal performance of the three measured ADPAs. Since the stand-alone main PAs operate similarly, the performance difference of the ADPAs results from the ξ-dependent modulation network. Compared to $\xi = 0.8$, $\xi = 1/N$ and $\xi = 1/\sqrt{N}$ achieve a larger bandwidth, higher gain and PAE. Overall, $\xi = 1/N$ has the best performance.

Possible reasons for the disagreement between the theory of section "Analysis of the asymmetric Doherty modulation network with a scaled impedance transformer" and the measurement results are losses of gain and bandwidth in the OMNs and impedance mismatch caused by process variations. Based on the Doherty impedance for the main amplifier $\underline{Z}_M$ mentioned in Table 1, an impedance transformation ratio of 12.3 ($\underline{\alpha} = 0$) and 2 ($\underline{\alpha} = N - 1$) for $\xi = 0.8$ is needed. For $\xi = 1/N$, the impedance transformation ratio is 6.2 ($\underline{\alpha} = 0$) and about 1 ($\underline{\alpha} = N - 1$), which makes it more robust against process deviations and model inaccuracies. A similar design on a thicker substrate (e.g. 512 µm) or different ϵ_r is suggested here to realize microstrip lines with higher characteristic impedances by wider, less process sensitive conductor paths.

Power-added efficiency in dependency of the probability density function

To benchmark the ADPAs, the averaging method with PDF weighting is used, as it was demonstrated in section "Drain efficiency depending on probability density function". Now the PAE is used instead of the DE as averaged value, which includes the gain performance of each amplifier. To compare all three ADPAs, the peak output power is lowered by 1 dB to 41 dBm with an observed bandwidth of 400 MHz reaching from 3.4 GHz to 3.8 GHz. This corresponds to a relative bandwidth of 11%. By lowering the peak output power by 2 dB to 40 dBm, a broader bandwidth of 900 MHz (3.2 GHz to4.1 GHz) can be used. Hence, the calculation of the averaged PAE is done for a fractional bandwidth of 25%. The results are shown in Table 3 with the highest $PAE_{PDF,B}$ for $\xi = 1/N$ for both cases.

Using the initially specified peak output power $P_{out,peak} = 42$ dBm within a 400 MHz bandwidth from 3.5 GHz to 3.9 GHz a $PAE_{PDF,B}$ of 38.8% for $\xi = 1/N$ can be achieved.

Table 2. Measured large signal performance comparison between ADPAs with different values of ξ.

ξ	$1/N$	$1/\sqrt{N}$	0.8
f (GHz)	3.3–4.1	3.3–4.1	3.4–4.0
P_{out} (dBm)	41–42	41–42	41–42
G_P (dB)	8.2–11.6	7.9–11.3	8.0–10.3
PAE_{PEP} (%)	52–63	46–63	50–58
PAE_{OBO} (%)	26–46	25–46	24–41
BW (%)	21.6	21.6	16.2

Table 3. Averaged power-added efficiency for Rayleigh-distributed signals with $N = 2.5$ at (a) $P_{out,peak} = 41$ dBm, $f_{min} = 3.4$ GHz, $f_{max} = 3.8$ GHz and (b) $P_{out,peak} = 40$ dBm, $f_{min} = 3.2$ GHz, $f_{max} = 4.1$ GHz.

ξ	$1/N$	$1/\sqrt{N}$	0.8
$PAE_{PDF,B}$ for (a)	37.9%	36.3%	33.3%
$PAE_{PDF,B}$ for (b)	30.1%	27.5%	25.2%

Power-added efficiency with modulated signals

In order to gain a more operation-related performance, comparison of the ADPAs measurements with modulated signals was carried out. The utilized baseband signal with a bandwidth of 50 MHz, a 256QAM modulation scheme and an EUTRA/LTE

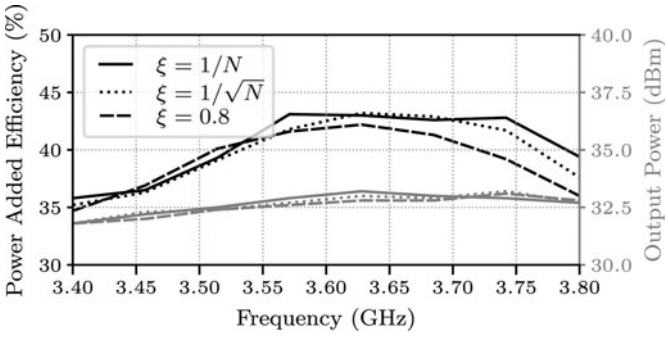

Fig. 15. Measured power-added efficiency and averaged output power for modulated baseband signals with a 50 MHz bandwidth, a 256QAM modulation scheme and an EUTRA/LTE baseband filter over carrier frequency for the ADPAs with $\xi = 1/N$, $1/\sqrt{N}$, and 0.8.

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Table 4. Performance comparison with state-of-the-art GaN HEMT Doherty power amplifiers for $\xi = 1/N$.

Ref.	f (GHz)	P_{out} (dBm)	G_P (dB)	PAE_{peak} (%)	PAE_{OBO} (%)	OBO (dB)	BW (%)	Board area (cm^2)
[11]	1.32–2.05	41.5–42.4	10.0–13.0	61.6–66.7[a]	49–52.5[a]	8.9	41	77[b]
[12]	2.0–2.6	43.8–45.4	8.0–11.0	36–68[a]	34–43[a]	8	26	64[b]
[2]	1.7–2.7	42.1–45.3	–	45–55[c]	41–55[c]	5–6	45	47[b]
[4]	2.8–3.55	43.0–45.0	8.3–9.1	55.8–63.5	42.8–53.0	6	23.6	56[b]
[13]	2.9–3.3	43.9–44.7	8.0–11.0	59.0–61.5[a]	39.5–40.5[a]	10	12.9	48[b]
[14]	3.0–3.6	43.0–44.0	6.0–11.0	46.2–54.9[a]	30.2–48.2[a]	6	18.1	110[b]
[15]	4.7–5.3	39.0–39.5	7.0–8.2	43.5–47.8[a]	24.9–27.7[a]	9	12.0	45[b]
This	**3.3–4.1**	**41.0–42.0**	**8.2–11.6**	**52.0–63.0**	**26.0–46.0**	**8**	**21.6**	**18.5**

[a]PAE calculated from given G_P and DE curves, $PAE = DE \cdot (1 - 10^{-G_P/10})$.
[b]DE, no PAE and no G_P curves are denoted.
[c]Estimation from given hardware photograph.

baseband filter leads to a PAPR of 7.9 dB. These baseband specification was chosen as example for a 5G signal transmission scenario. The PAE was measured for carrier frequencies swept from 3.425 GHz to 3.775 GHz, while keeping the average output level around 32.5 dBm. The measurement results are shown in Fig. 15. Here it becomes evident that the ADPA with $\xi = 1/N$ achieves the highest PAE for carrier frequencies higher than 3.7 GHz. Furthermore, this ADPA version has the highest PAE performance of 41%, as averaged over the measured frequency range. The ADPAs with $\xi = 1/\sqrt{N}$ and $\xi = 0.8$ reach a slightly lower averaged PAE of 40% and 39%, respectively. These results also confirm the trend calculated in the previous subsection "Power-added efficiency in dependency of the probability density function".

Conclusion

To classify the achieved performance, the circuit is compared with similar publications in Table 4. For this purpose, symmetric and asymmetric architectures with enhanced fractional bandwidth (BW) are considered.

To the authors' knowledge, no similar work has been published that investigates the broadband effect of the main amplifier's IT for an ADPA. The considerations in section "Analysis of the asymmetric Doherty modulation network with a scaled impedance transformer" extend the existing state-of-the-art theory on ADPAs and provide an enhanced approach for a more energy-efficient circuit design.

A major field of application for DPAs are massive MIMO base stations for latest and future mobile standard communications. Due to the large number of devices and limited space in such base stations, the occupied board area is of great importance. In this work, the by far most compact amplifier design was demonstrated. The achieved board area is smaller by a factor of 2.3 compared to the next smallest design. The use of a discrete hybrid coupler at the input as well as the avoidance of long microstrip lines have proven to be very beneficial.

For the purpose of this comparison we focused on the amplifier with $\xi = 1/N$, since it has the best performance. The obtained PAE_{peak} of 52.0% to 63.0% at peak power is roughly the same as in [4, 11–13]. However, those circuits are operating at lower frequencies. The study in [4] uses the same active component, but is designed for a higher output power and utilizes a higher drain voltage. This is beneficial for an efficient operation due to a lower impact of the knee voltage. For an ADPA with an OBO larger than 6 dB and a center frequency higher than 3.0 GHz, the highest PAE performance is achieved with this work. To reach such a high PAE, sufficient operating gain has to be ensured. In this work, we demonstrated the highest value of 8.2 dB to11.6 dB for center frequencies above 2 GHz.

The comparison with the state-of-the-art emphasizes that the proposed design approach is a suitable solution for efficient broadband power amplifiers with a high dynamic range. The intrinsic node matching turns out to be a promising method to ensure an efficient PA design. The maximum broadband matching at $V_{in,\xi}$ can be applied for transistors with different output impedance or for different values of Z_0 with an additional post matching network in the future. However, to meet an efficiency optimized operation for signals with high PAPR and instantaneous bandwidth, matching at the expected value is beneficial.

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