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Electron Microscopy and Spectroscopy Characterization of the Effects of Annealing on the Cu/Graphene/Si Multilayer Thin Films

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Graphene, a single-atomic-layer of carbon with a hexagonal lattice structure, has outstanding electrical and mechanical properties as well as excellent thermal and chemical stabilities. This makes graphene as a potential candidate as an atomically-thin diffusion barrier for Cu interconnects in back-end-of-line (BEOL) processes in Si integrated circuit technologies [1]. To explore graphene's capability for this technological application, presented here is a comparative study of the effects of annealing on the Cu/Graphene/Si multilayer thin film and the Cu/Si thin film.

The graphene used in this study was synthesized in a custom built inductively coupled plasma chemical vapor deposition (ICPCVD) on a 50 nm thick Ni/Au alloy catalyst, with composition of 99 wt.% Ni and 1wt.% Au. The graphene was synthesized at 500°C by flowing in 0.1 sccms of carbon precursor(C_2H_2) at 10 watts of plasma for 30 seconds. After the ICPCVD growth, the graphene was transferred to a clean p doped silicon substrate with native oxide layer of less than 3 nm. Following the transfer process, 200 nm of Cu layer was deposited on top of the graphene using dc magnetron sputtering, the sample referred to as Cu/Graphene/Si. For the purpose of comparison, Cu was directly deposited onto a Si substrate at the same thickness, the sample referred to as Cu/Si. The samples were annealed at 300°C, 400°C, 500°C and 600°C for 30 minutes, respectively, and characterized by transmission electron microscopy (TEM) with an energy dispersive X-ray spectrometer (EDX). X-ray diffraction (XRD) characterization was carried out to examine phase changes that may have occurred upon annealing at different temperatures.

Figure. 1 (a) shows TEM bright-field (BF) micrograph of Cu/Si after 300°C annealing for 30 minutes. As seen in figure, the Cu layer has reacted with the Si substrate to form a thick layer of Cu_3Si at the interface. The presence of Cu_3Si formation at the interface was confirmed by the EDX spectrum as shown in Figure. 1 (d), where both Cu and Si X-ray peaks were identified in the area highlighted in Figure.1 (a). The XRD patterns in Figure. 1 (g) obtained from the same sample indicate that without graphene as a diffusion barrier, the Cu/Si interface can easily react to form Cu_3Si at temperature of 300°C and above.

Figure. 1 (b) is a TEM BF micrograph of the Cu/Graphene/Si after annealing at 300°C for 30 minutes. The image shows a well-defined interface between Cu and Si with an unreacted 200 nm thick Cu layer. Figure. 1 (c) is a high resolution TEM micrograph obtained from the area indicated by the box in Figure. 1(b). The parallel lattice fringes highlighted in Figure. 1 (c) shows a pristine 3-4 layers graphene at the interface of Cu and Si. The XRD spectra in Figure. 1 (h) show that the graphene at the interface prevented Cu diffusion into Si under thermal annealing up to 500°C. However, when annealed at 600°C for 30 minutes, the corresponding XRD pattern in Figure. 1 (h) shows presence of Cu_3Si peaks indicating failure of the graphene as a barrier. This preliminary study shows that a low temperature grown multilayer

graphene can serve as an excellent copper diffusion barrier up to 500°C of annealing. TEM, EDX, and XRD are powerful tools to study diffusion barrier properties of graphene. A systematic investigation into the effects of defect density and the layer number of a low temperature grown graphene in relation to its capability of serving as a diffusion barrier at different annealing temperatures is ongoing [3].

References:

[1] B.S. Nguyen, J.F. Lin, D.C. Perng, Appl. Phys. Lett., Perng. 104, 082106 (2014)
[2] J.Hong, S.Lee, S. Lee, H. Han, C. Mahata, H.W. Yeon, B. Koo, S. Kim, T. Nam, K. Byun, B.W Min, Y.W. Kim H. Kim, Y.C. Joo, T. Lee. Nanoscale. 6, 7503 (2014).
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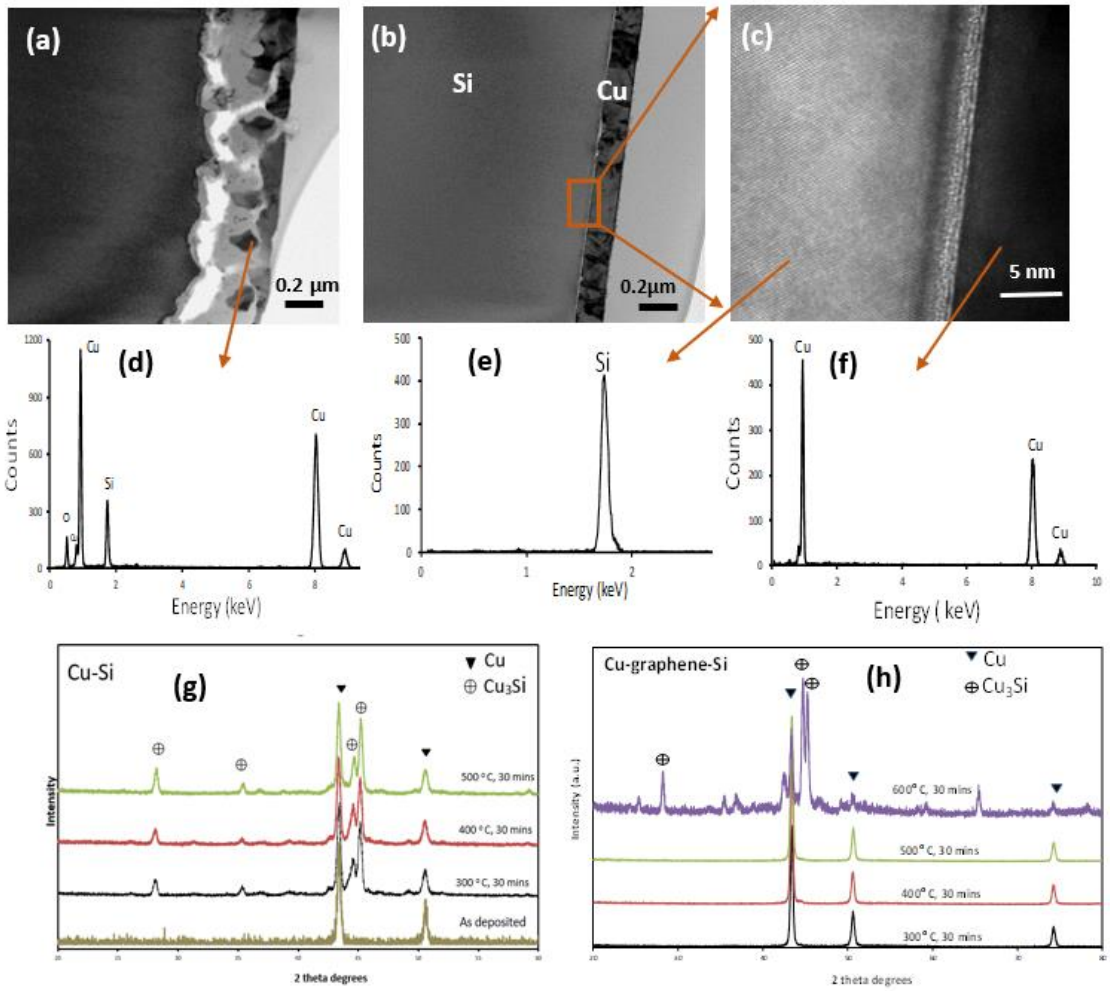

Figure. 1 (a) and (b) show TEM bright-field (BF) micrograph of Cu/Si and Cu/graphene/Si after annealing at 300°C for 30 minutes respectively. (c) is a high resolution TEM image taken from the area shown in the box in Figure (b). Figure (d) shows EDX spectra taken at the interface of Cu-Si sample at 300°C showing presence of Cu and Si peaks, Figure (e) and (f) show EDX spectra from Silicon substrate and Copper thin film, respectively. Figure (g) and (h) show XRD spectra taken after annealing Cu-Si and Cu-graphene-Si samples at elevated temperatures, respectively.

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