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Xe plasma FIB Delayering of IC based on 14 nm node technology

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The burgeoning generation of electronic data and the growing need for fast processing is driving the development of unique architectures in microelectronic devices. High device performance, along with low energy consumption, decreasing device area and optimal production costs are the four basic tenets of operation in the microelectronics industry [1]. These rules have led to ever-increasing area density of the basic elements in electronic devices and consequently to shrinkage of the elements to the nanometer scale. This has brought new challenges for production technologies as well as for failure analysis of such devices.

State-of-the-art commercial electronic devices are based on 22 nm and 14 nm node technology and the next generation of 10 nm and 7 nm nodes are under development [1]. These technologies call for unique instruments and workflows for the identification and excavation of nanometer-sized faults buried under the device surface. Mechanical polishing as a standard tool in the failure analysis process does not meet the very strict requirements of these state-of-the-art nodes. The thickness of metal interconnects and dielectric separating layers just above the transistors has shrunk to less than 100 nm. Therefore it is a challenge to stop the polishing process in a particular layer with the expected quality, accuracy and repeatability. Moreover, mechanical polishing is usually accompanied by surface artefacts like material chipping-off and site-specific fault excavation is usually impossible. Focused Ion Beam (FIB) technology has proven to overcome these restrictions. It offers the possibility to target a failure with nanometer accuracy in depth as well as in the lateral direction. Therefore cross-sectioning, site-specific layer-by-layer excavation (also known as delayering) and direct extraction of a Transmission Electron Microscopy (TEM) lamella containing the particular fault of interest have become standard methods in failure analysis.

In this contribution we present delayering of an Intel Skylake processor (G4400) based on 14 nm node technology [2]. The delayering is performed with a Xe plasma focused ion beam. Beam currents of Xe FIB up to 2 µA has extended the dimensions of the analyzed volume of interest to several hundred micrometers in general [3, 4] while simultaneously enabling homogeneous delayering with nanometer accuracy. Xe FIB is advantageous also because interaction of inert Xe atoms with the material surface does not significantly alter either the properties or the reactivity of the material and the ability of Xe to induce surface contamination is negligible. Moreover Xe ions considerably reduce surface amorphisation when compared to Ga ions [5].

Processor architecture is based on alternating metal and dielectric layers (Fig. 1). These layers have different sputtering rates when FIB delayering is applied. Uneven sputtering can be substantially suppressed by chemical means. In our experiments, water vapor was delivered directly to the point of patterning via a Gas Injection System (GIS) in order to equalize sputtering of metal interconnects and insulators. The result of processor delayering down to the first metal layer, just above the transistors is shown in Fig. 2. The damage-free surface of the transistor contact layer is ready for electrical probing.

Nanometer-sized elements in state-of-the-art electronics have posed a challenge also for imaging technologies. Clear observation of the very thin individual layers means suppressing the acceleration voltage of primary electrons to the sub-1 kV range, ideally to 500 V. At higher energies, the electron signals from different layers would intermix as they are generated in a volume comparable to the thickness of those layers. However, sub-nm resolution at low electron energies is a necessary condition due to the size of the observed features. High resolution pictures captured at 500 V are shown in Fig. 2. Low-kV imaging has verified highly homogeneous delayering of the processor as can be seen by the absence of large contrast changes in the delayered region.

[1] http://www.itrs2.net/
[2] http://www.intel.com/content/www/us/en/silicon-innovations/intel-14nm-technology.html
[3] T Hrnčíř et al, 38th ISTFA Conf. Proc. (2012), p. 26.
[4] A Delobbe et al, Microsc. and Microanal. 20 (2014), 298.
[5] T Hrnčíř et al., 41th ISTFA Conf. Proc. (2015), p. 60.

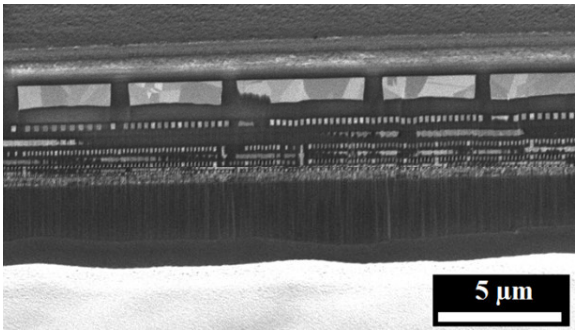

Figure 1. Intel® Pentium® Processor G4400 (Skylake, 14 nm node) after mechanical polishing and Xe FIB cross-sectioning.

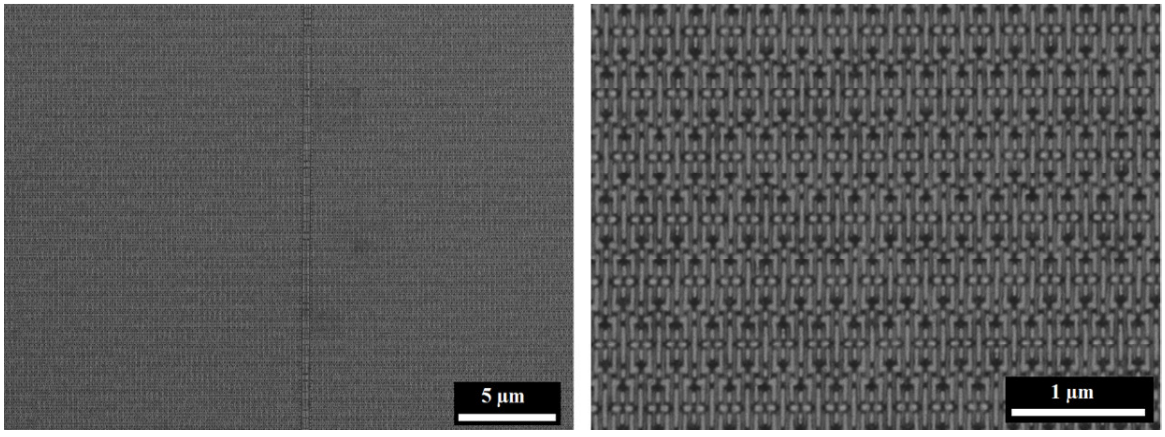

Figure 2. Top view of the transistor contact layer in a commercial Intel® Pentium® Processor G4400 (Skylake, 14 nm node) after the delayering process in a TESCAN XEIA3 FIB-SEM system. A global overview (left) and close-up micrographs (right) are taken with a SE detector at 500 V using beam deceleration mode.

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