Probing Nanoscale Local Lattice Strains in Semiconductor Nanostructures and Devices by Transmission Electron Microscopy

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Strain is an important parameter for understanding the mechanical and electronic properties of materials and devices, whether this strain is intrinsic or applied. Strain engineering of semiconductors has become an important method for altering the structural, electronic, and optical properties of materials. Today's microprocessors, for instance, utilize strained silicon channels to enhance the charge carrier mobility. Strain-induced polarization fields in Group III-V quantum well structures play an important role in the emission characteristics of light emitting diodes. Strain compensated super-lattice structures are used to improve crystal growth and achieve higher quantum efficiencies in photocathode diodes. The continuous scaling of the active regions of these devices requires characterization techniques with nanometer scale resolution to assist the development of new material processing methods [1].

Among the various techniques that can be used to measure strain such as X-ray and neutron diffraction or Raman spectroscopy, transmission electron microscopy (TEM) is the only tool capable of measuring strain at the nanometer scale. For improved spatial resolution, transmission electron microscopy (TEM) based techniques such as Moire interference, convergent beam electron diffraction (CBED), nano-beam electron diffraction (NBED), strain mapping from either real space analysis or the geometrical phase analysis (GPA) of high resolution (scanning) transmission electron microscopy ((S)TEM) images, and dark-field electron holography (DFEH) have been developed and used to provide information about the strain in semiconductor devices.

In this report, we summarize our recent studies on nanoscale local lattice strains measurement in advanced Si CMOS devices, metal-oxide-semiconductor field effect transistors, and shallow trench isolation liners by CBED; and the investigation of local strain and core structure of Lomer dislocations in CdTe by using GPA of the experimental HAADF-STEM images. These strain fields will affect the electrical and electronic properties of semiconductors by distorting the local bonding character. Also, we have performed strain analyses on semiconductor devices and compared the precision and resolution of different TEM based strain measurement methods such as CBED, NBD, HRTEM & HR-STEM GPA DFEH and SMF.

Shown in Figure 1 are [340] zone axis CBED patterns of poly-Si/TiN/HfO$_2$/SiO$_2$/Si stacks with the TiN layer thickness of 3 and 20 nm in (a) and (b), respectively. Scaling of TiN thickness was found to be effective both in increasing tensile stress on Si substrates and in lowering the effective workfunction (EWF) of metal gate nMOSFETs. TiN-induced strain was found to be the primary reason for the electron mobility enhancement.

Figure 2(a) shows HAADF STEM image of a Lomer dislocation core at a [1-10]/(110) 2° tilt CdTe GB fabricated by wafer bonding. It is a 60° dislocation with two distinct extra planes separated by a 1~2 atomic plane distances which could be clearly seen from the strain map of the in-plane ε_{yy} calculated by

the GPA (b). The importance of understanding the atomic structure and electronic behavior of such defects in elemental and compound semiconductors has long been recognized by the PV community [5].

References:

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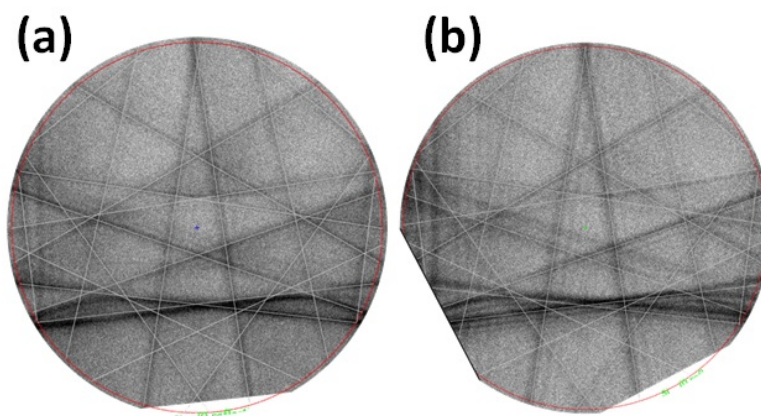
Figure 1. CBED patterns from poly-Si/TiN/HfO$_2$/SiO$_2$/Si stacks with the TiN layer thickness of 3 and 20 nm in (a) and (b). (a) Thicker film with ε_{yy} = .13% and ε_{zz} = .04%. (b) Thinner film with ε_{yy} = .44% and ε_{zz} = .42%.
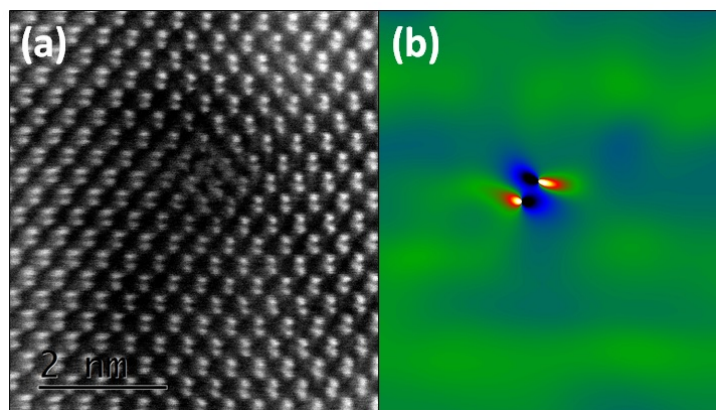
Figure 2. (a) HAADF STEM image of a Lomer dislocation core at a [1-10]/(110) 2° tilt CdTe GB fabricated by wafer bonding, (b) strain map of the in-plane ε_{yy} calculated by the GPA.