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Research Paper

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Abstract

We present a self-biased three-stage GaN-based monolithic microwave integrated circuit low-noise amplifier (LNA) operating between 26 and 29 GHz for 5G mobile communications. The self-biasing circuit, common-source topology with inductive source feedback, and RLC negative feedback loops between gate and drain of the third transistor were implemented to achieve low noise, good port match, high stability, high gain, and compact size. Measurement results show that the LNA has a high and flat gain of 30.5 ± 0.4 dB with noise figure (NF) of 1.65–1.8 dB across the band. The three-stage topology also achieves high linearity, providing the 1 dB compression point output power (P_{1dB}) of 21 dBm in the band. To our knowledge, this combination of NF, gain, and linearity performance represents the state of art of self-biased LNA in this frequency band.

Introduction

The first 5th generation (5G) mobile network was rolled out in South Korea in 2019. Compared to the previous generations, 5G provides much higher capacity and lower latency to meet the requirements of ever-increasing data rate, number of connected devices, and emerging applications. To achieve this, wider bandwidth and more frequency bands have been assigned to 5G including sub-6 GHz bands and millimeter-wave (mm-wave) bands such as 26–30 GHz [1, 2]. Although mm-wave can provide a chunk of continuous bandwidth up to GHz, only a few countries have adopted it in reality; most deployed 5G networks are running at sub-6 GHz bands. One of the major challenges for deploying mm-wave 5G lies in the immature technology for frontends, causing low gain, low power efficiency, and high cost. Low-noise amplifiers (LNAs) are critical components in the frontend of all communication systems usually located at the first stage of the receiver after the antenna. Typical semiconductor technologies for LNAs are divided into two categories: silicon and III–V compound. The former includes complementary metal oxide semiconductor (CMOS), silicon germanium bipolar complementary metal oxide semiconductor (SiGe BiCMOS), and silicon on insulator which have the advantages of low power consumption, high integrability, low cost, and compact size but is poor with regard to noise figure (NF) and gain [3, 4]. The latter consists of conventional Indium phosphide (InP) [5] and gallium arsenide (GaAs) [6] high electron mobility transistors (HEMTs) which have lower NF and higher gain than the silicon technologies. More recently, gallium nitride (GaN) HEMTs have received great attention for their excellent performance in both low noise and high power [7–9]. Compared with GaAs and InP, one of the significant advantages of GaN LNAs is their high-power handling capability which is preferable in complex electromagnetic environments, e.g., remote sensing in space or satellite communications, where additional measures, such as limiters, must be implemented to protect the receivers. In addition, the high-power tolerance ability is also desirable in signal detection and electronic countermeasure and multiple input multiple output communications [7].

In this work, we demonstrate a three-stage monolithic integrated GaN LNA operating between 26 and 29 GHz for mm-wave 5G applications. Unlike GaN LNAs reported elsewhere [10, 11], the LNA demonstrated here has three stages and is powered by a single power supply. Such a design simplifies biasing circuits and makes the whole circuit more compact. The measured gain and 1 dB compression point output power (P_{1dB}) are 30.5 ± 0.4 dB and 21 dBm, respectively. The NF is 1.65–1.8 dB in 26–29 GHz. The measured S_{11} and S_{22} are both below -10 dB across the whole band. The results show the proposed GaN LNA could be an ideal candidate for mm-wave 5G.

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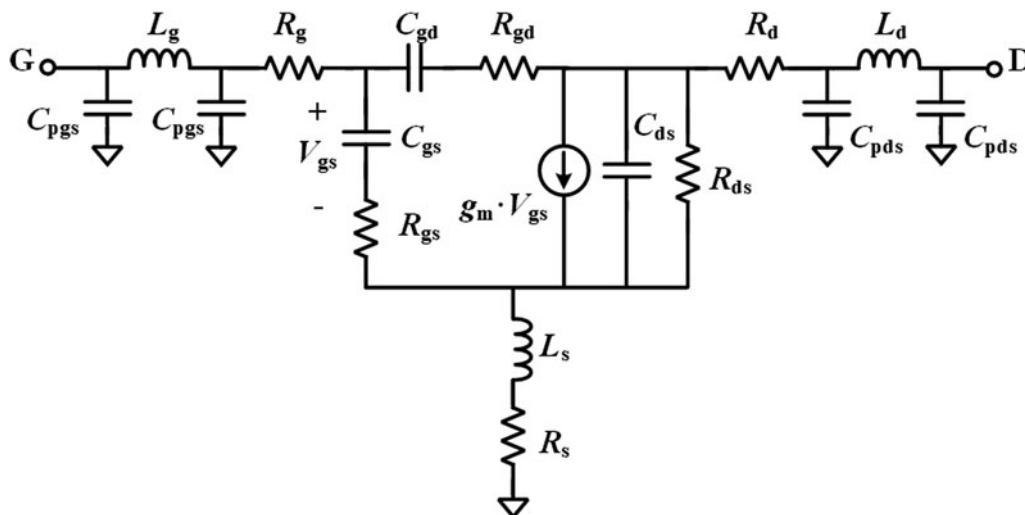


Fig. 1. The small-signal equivalent circuit of GaN HEMT when being biased at $V_g = -2$ V and $V_d = 15$ V.

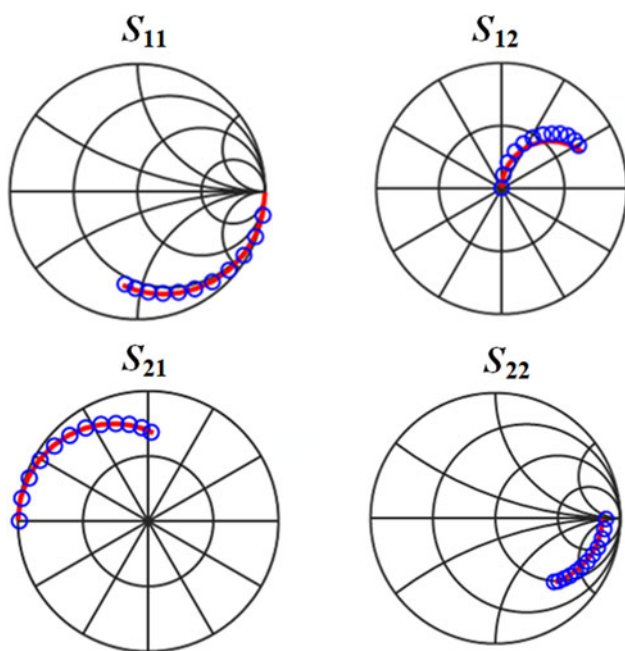


Fig. 2. The measured (blue circle) and modeled (red line) S-parameters. The frequency range is from 0.2 to 60 GHz.

LNA design

The HEMT and its small-signal model

The GaN transistor used in this work is $2 \times 30 \mu\text{m}$ and is developed using a $0.1 \mu\text{m}$ depletion mode. Figure 1 shows its small signal equivalent circuit. The initial bias conditions of the device were chosen to achieve the maximum value of $f_T \times g_m / I_{DS}$, where f_T , g_m , and I_{DS} are transition frequency, transconductance, and source-drain current, respectively [12–15]. However, the ultimate optimal bias voltages at the gate, V_g , and the drain, V_d , are -2 and 15 V, respectively. They were decided as a compromise among matching loss, NF, gain, and stability. In order to match the input impedance (Z_{in}) of the LNA to 50Ω , an inductive degeneration was adopted, making the real part of Z_{in} equal to $2\pi L_{seff} + R_s$, where L_{seff} is the

effective source or emitter inductance and R_s is the source resistance. The measured S-parameters of the transistor are shown in Fig. 2 and extracted values of the small-signal equivalent circuit are shown in Table 1. The simulated results based on the model are in good agreement with the measured ones.

LNA design

In this work, we used a common source cascaded three-stage architecture to achieve a minimum gain of 30 dB, which is higher than the state of art LNAs operating in the same frequency range, while keeping NF as low as possible as shown in Fig. 3. The overall NF in a cascaded system is determined by the well-known Friis equation

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} \quad (1)$$

where NF_x and G_x ($x = 1, 2, 3$) are NF and gain of the x th stage of the cascaded LNA in a linear scale. The gain and NF of the first stage are more important than those of the following stages. Since HEMTs are constructed in a common source topology and the same HEMTs are used for all stages, the main task is then focused on input matching for minimizing the NF and lowering the input return loss at the first stage. The final stage serves the purpose of maximizing gain, improving the flatness of the gain, and reducing output return loss. A series RLC negative feedback loop, highlighted in blue in Fig. 3, is applied between the gate and drain of the third stage to adjust the gain flatness and improve the stability. However, its contribution to the overall NF is very limited as seen in (1). The inter-stage is tuned to ensure noise, gain, and input and output standing wave ratio meet the overall goal. A feedback inductor was deployed at the source of the HEMT, to achieve minimum NF and low input return loss simultaneously as highlighted in green in Fig. 3. Adding this inductor at the first stage will rotate S_{11} of the LNA close to the optimum reflection coefficient Γ_{opt} for noise [10] and achieve both optimal noise matching and input conjugate matching [16]. Finally, the inductive source feedback can also improve the stability. Although the inductive degeneration does not have the same impact on the NF as resistive degeneration does, it still reduces the overall gain of the circuit.

Table 1. Extracted intrinsic small-signal parameters of the GaN HEMT

Intrinsic parameters	g_m (mS)	R_{ds} (Ω)	R_s (Ω)	R_d (Ω)	L_s (pH)	C_{gs} (fF)	C_{gd} (fF)
Value	84.5	192	22.9	64.9	5.8	47.9	5.1

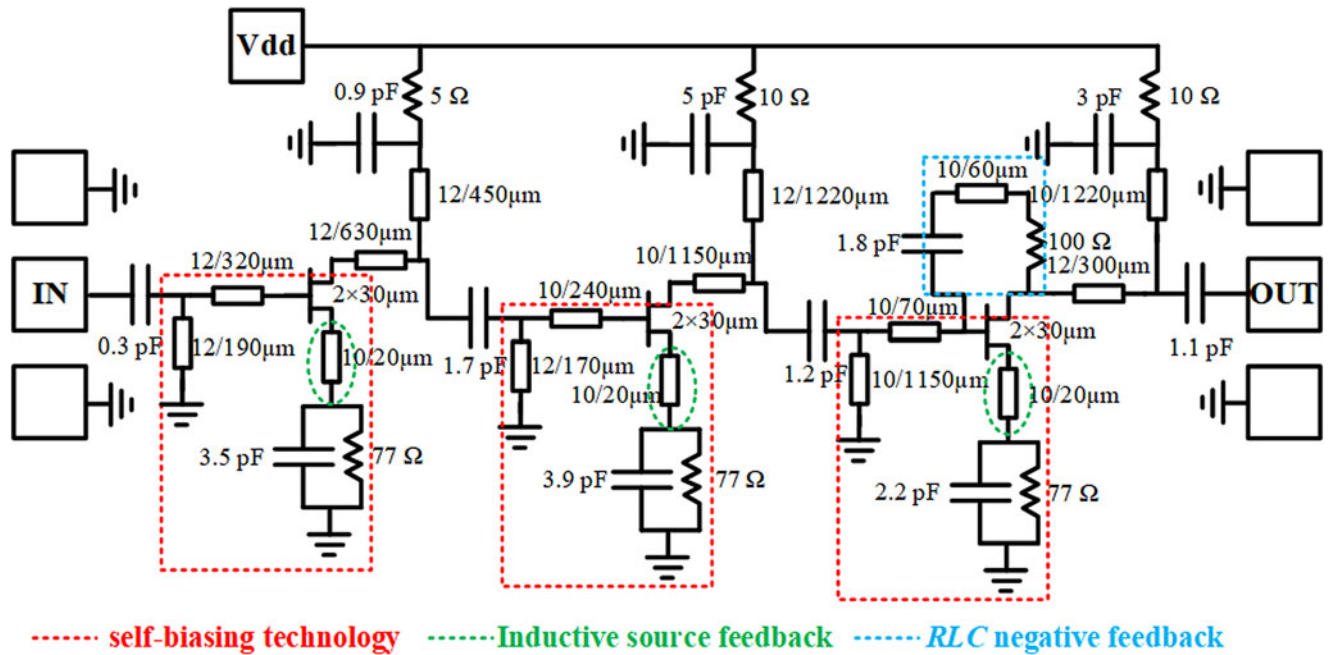


Fig. 3. Simplified schematic of the designed LNA.

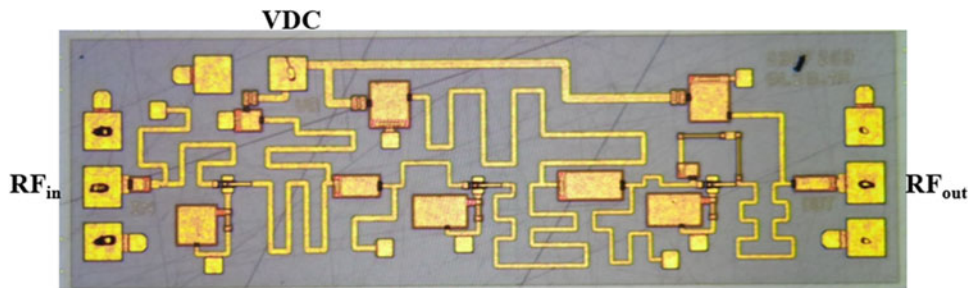


Fig. 4. Photograph of the fabricated LNA.

Biasing circuit

A self-biasing technology is utilized to power all HEMTs conveniently through a single drain voltage, providing greater flexibility of biasing conditions [17, 18]. As highlighted in red in Fig. 3, the circuit contains a shunt resistor (R) and capacitor. The capacitor acts as a bypassing capacitor, helping to filter out noise contribution from the feedback resistor and improve the gain at the interested frequency range. The negative voltage on the resistor (R) is supplied to the gate through the grounded microstrip of the input matching circuit that, as part of source impedance matching, simplifies the input matching network, thus V_g can be expressed as $-I_{DS} \times R$. In the proposed LNA, I_{DS} and R are 25.9 mA and 77 Ω , respectively, when it is biased at $V_g = -2$ V and $V_d = 15$ V. Although careful design and several iterations of process validation have been made, the process variation may still

affect the self-biasing circuit. In fact, we implemented a laser trimming on the resistor for fine-tuning. It should be noted that, due to the presence of the capacitor, much more care should be taken for stability simulation. A quarter-wavelength stub with a resonant capacitor and a resistor in the drain bias line is used as a radio frequency (RF) choke for stability improvement at each stage. Furthermore, the whole circuit has only two bonding pads for the drain, which can largely ease bonding and packaging. The overall bias circuits are more favorable for practical applications.

Measurements and discussion

Figure 4 shows the fabricated monolithic microwave integrated circuit (MMIC) LNA that has an area of 0.8×2.4 mm².

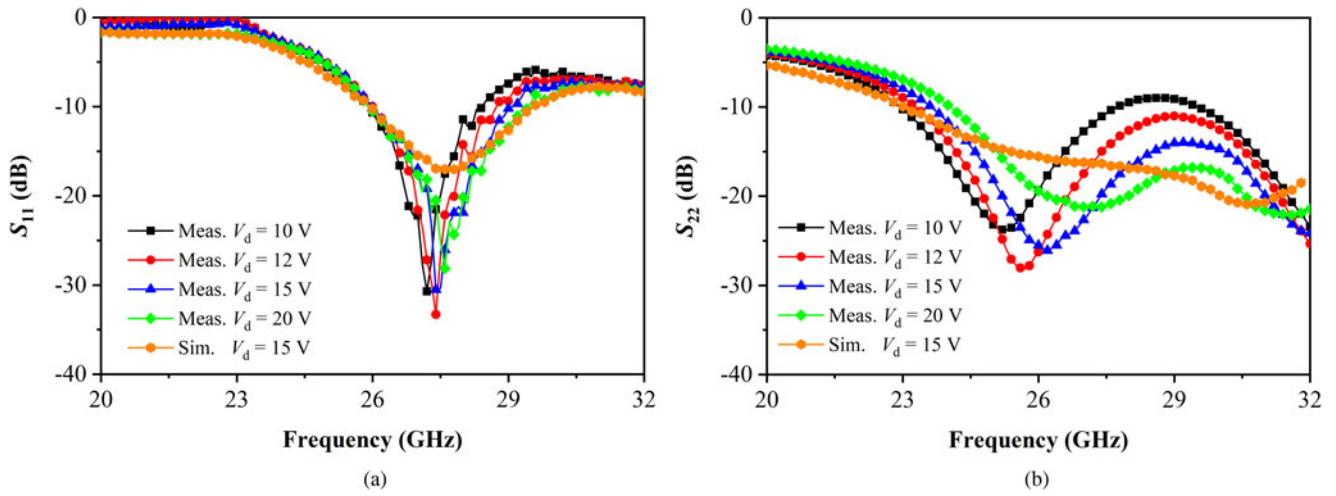


Fig. 5. Measured and simulated S_{11} (a) and S_{22} (b) of the LNA at different bias points.

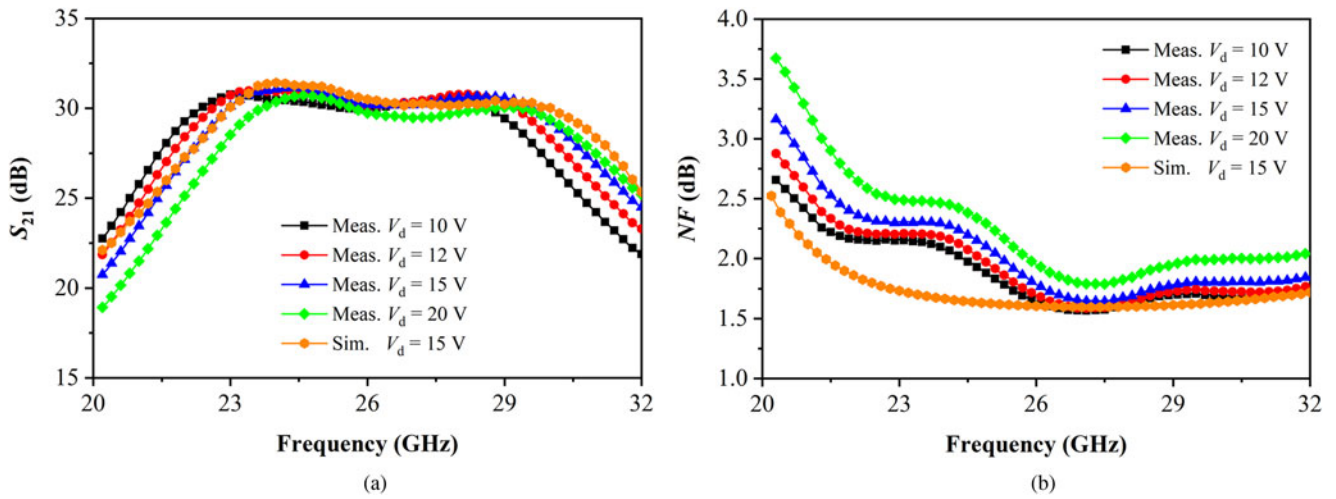


Fig. 6. Measured and simulated S_{21} (a) and NF (b) of the LNA at different bias points.

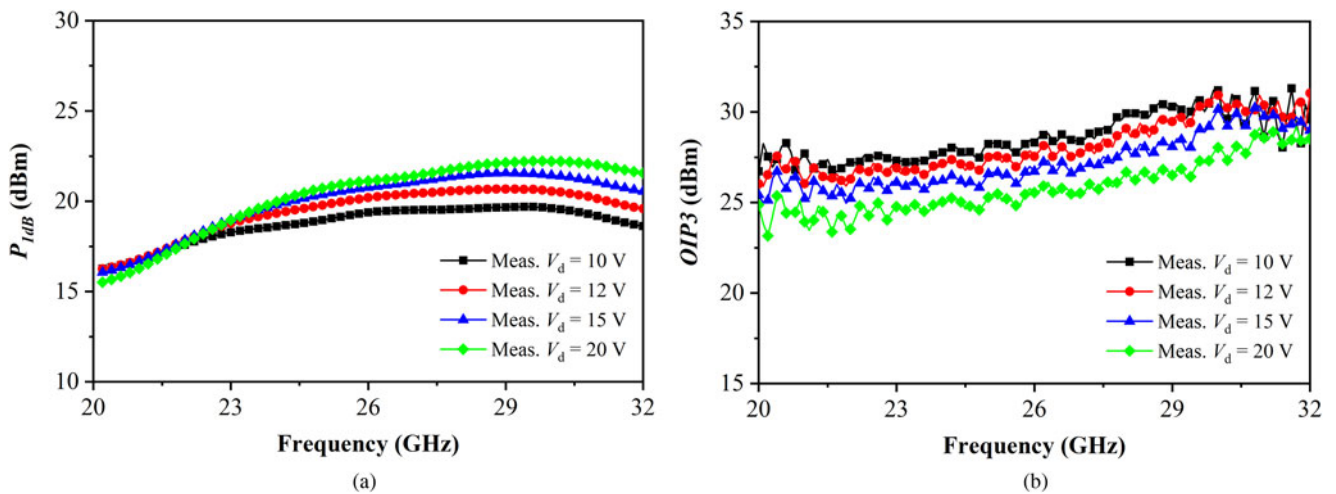


Fig. 7. Measured P_{1dB} (a) and OIP3 (b) of the LNA at different bias points.

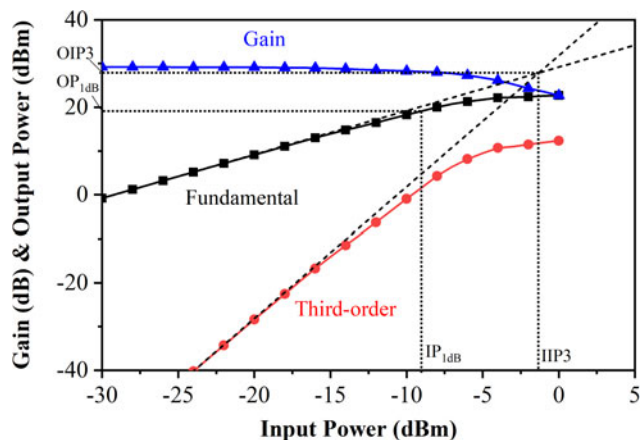


Fig. 8. Measured gain and output power versus input power at 28 GHz ($V_d = 15$ V, with RF and direct current (DC) pads bonded to the test board).

Although -2 and 15 V are required for gate and drain of the HEMT, only 15 V was needed because a self-biasing technology was adopted. S-parameter measurements were made on chip with ground-signal-ground probes at room temperature and the results are shown in Figs 5 and 6. As can be seen, the measured S_{11} and S_{22} are below -10 dB between 26 and 29 GHz, indicating that both the input and output matching are good. Moreover, the measured gain is 30.5 ± 0.4 dB in the same frequency range. The simulated results are also plotted against the experimental results, and good agreements have been achieved. The cold source method was used to measure NF and both the experimental and simulated results are shown in Fig. 6(b). One can notice that the measured NF is between 1.65 and 1.8 dB in the band, and the discrepancy between the measurement and simulation is smaller than 0.3 dB. The linearity of the LNA was also investigated and the results are shown in Fig. 7. The measured P_{1dB} and third-order intercept point output power (OIP3) are approximately 21 and 27 dBm, respectively, which are much higher than GaAs and InP LNAs. Figure 8 shows the measured gain and output power versus input power at 28 GHz when the LNA is biased at $V_d = 15$ V. Note that the measured OIP3 and the results in Fig. 8 were obtained after the chip was packaged, which are slightly lower than the results obtained by on-chip measurements due to bondwire and packaging.

The analysis of the fabricated LNA is also performed at different bias points (10–20 V) as shown in Figs 5–7. It is observed that the device performs better in terms of return loss and gain at lower drain voltage and the gain ripple remains the same for all the cases. The designed LNA gives promising results to all four bias conditions. It is noticed that the LNA can accommodate a wide range of supply voltages from 10 to 20 V, which is preferred in radar systems in practice.

We compared the performance of the designed LNA with recently published LNAs using different semiconductor technologies for mm-wave 5G and the results are summarized in Table 2. We can observe that NF of this work is comparable with InP LNAs, even better than GaAs and CMOS. Moreover, it is noteworthy that the single power supply employed in this work can ensure a competitively excellent performance compared with the other works powered by dual sources using the same technique. It is known that the main drawback of the self-biasing technique is sacrificed gain and NF. In addition, this LNA has a relatively high and flat gain as well as a high P_{1dB} of 21 dBm compared to GaAs and InP LNAs. Meanwhile, the high linearity sacrifices the power consumption but is still much higher than LNAs using other technologies. The measured NF is slightly higher than that of other LNAs based on 0.1 μ m GaN process due to the resistors in the self-biasing circuits. However, the adopted self-biasing structure simplifies external circuitry.

Conclusion

A GaN LNA based on 0.1 μ m GaN MMIC process operating at 26–29 GHz is demonstrated in this work. The single powered LNA has a high and flat gain of 30.1–30.9 dB and good input and output matching. The NF is 1.65–1.8 dB in the band. The LNA has good linearity with P_{1dB} close to 21 dBm. Compared with the published LNAs, the LNA demonstrated in this work exhibits a competitive NF and a relatively high and flat gain as well as high linearity. In addition, this single powered LNA provides ease of use and simplifies the overall system on account of the powering method compared to that of the individually powered LNA. To our knowledge, the combination of NF, gain, and linearity performance represents the state of art of self-biased LNAs suitable for mm-wave 5G communications.

Table 2. Comparisons of LNAs for mm-wave 5G using different semiconductor technologies

Ref.	Tech.	Freq. (GHz)	Gain (dB)	NF (dB)	P_{1dB} (dBm)	Size (mm ²)	P_{DC} (mW)
[5]	0.1 μ m InP	26–40	21–22.8	1.3–1.9	NA	2.1 \times 0.82	14
[11]	0.15 μ m GaN	27–31	15–20	3.7–3.9	NA	1.2 \times 3.4	280
[6]	0.15 μ m GaAs	25–40	18.7–21.7	2.2–2.8	NA	2.5 \times 1.2	230
[19]	65 nm CMOS	25–30	17–21	>3.7	NA	0.2 \times 0.85	10
[20]	130 nm CMOS	26.3–28	17–20	5.2–7.5	NA	0.27	24
[4]	22 nm FD-SOI CMOS	26.6–31.6	16–19.3	4.8–5.2	-18	0.705 \times 0.38	11.4
[10]	0.1 μ m GaN	23–31	22–27.5	0.93–1.4	22–25	1.9 \times 0.8	NA
This work	0.1 μ m GaN	26–29	30.1–30.9	1.65–1.8	21	2.4 \times 0.8	1165

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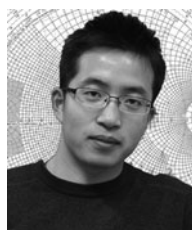
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components, systems and metrology, and next-generation wireless communications.



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