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Microstructure and Electrical Properties of III-As Gate Stacks with Amorphous Rare-Earth High-k Oxides

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Integration of group III-V semiconductors, such as InGaAs due to its excellent electron transport properties, with high-k dielectrics is a possible option for the realization of low power, high performance MOSFETs for 15 nm technology node and beyond [1]. Amorphous oxides, such as $Ga(Gd)_2O_3$ and Al_2O_3, have demonstrated so far the best interfaces with GaAs and InGaAs and as a result excellent transistor characteristics, but they have relatively low dielectric constant making scaling difficult. More common, HfO_2 and ZrO_2 gate oxides are typically formed in a polycrystalline form resulting in increased leakage and, possibly, higher trap density due to grain boundaries. Rare-earth ternary oxides ($LaAlO_3$ or $GdScO_3$) have stable amorphous phase up to 1000 ^{0}C and relatively high dielectric constant (17 and 23, respectively), and are quite promising as novel gate oxides. One of the potential approaches to this gate stack integration involves an amorphous Si interface passivetion layer (IPL) which has proven to reduce interface trap density and gate leakage current, to improve thermal stability of the interface properties and in some cases to reduce the gate oxide charges [2].

The focus of the paper is on correlation of chemistry, microstructure and electrical characteristics of gate stacks with amorphous rare-earth oxides and Si IPL on GaAs and InGaAs and there thermal stability, which is essential in MOSFET processing. The gate stacks were fabricated using molecular beam epitaxy (MBE) and in-situ deposition of amorphous Si IPL and quasi-in-situ (with protection layer deposition and desorption) MBE of high-k oxides [3]. TEM with EDX and EELS accompanied with XPS was used for microstructural and chemical analysis, and capacitance-voltage and transistor characteristics were measured on processed test structures.

The $LaAlO_3$/GaAs stack with *a*-Si IPL (which is oxidized within process flow) exhibited not only excellent thermal stability of the electrical and structural properties up to 800 ^{o}C (Figs. 1-3), but demonstrated a reduction of EOT by ~50% (Fig. 3) with annealing, 20-fold reduction of hysteresis, and interface state density as low as 2×10^{11} $eV^{-1}cm^{-2}$ [3]. Oxidation of the Si IPL were studied to ensure that no covalent Si is available for diffusion into semiconductor [4]. The observed dissolving of low-*k* SiO_x layer into $LaAlO_3$ at higher temperatures (Fig.2) can explain increasing of accumulation capacitance and reduction of the equivalent oxide thickness (EOT) with annealing shown in the Fig. 3. Similarly, excellent thermal stability is found in the $GdScO_3/SiO_x$/ InGaAs/InP stack (Fig. 4,5). Although the $GdScO_3/SiO_x$ interface appears very stable, the Ni/$GdScO_3$ interface has shown catalytically-induced Gd_2O_3 crystallization with associated $GdScO_3$ phase separation (Fig. 4). This gate stack demonstrated record low frequency dispersion (< 5%/dec.) in accumulation for InGaAs channel material (Fig. 5), reduced fixed oxide charge leading to a positive shift (~0.5V) of flat band voltage, reduced interface trap density close to the valence band, although D_{it} was higher at midgap. All the gate stacks with *a*-Si IPL have shown significant reduction of gate leakage current after annealing. Fig. 5(bottom) shows input characteristics of enhancement mode InGaAs/InP n-MOSFET (V_T=0.3 V) with subthreshold slope of 130 mV/dec., Ion/Ioff ~ 10^5, and channel resistance in the linear region 1.5 kΩ/sq. [5].

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[5] This research was supported by the SRC/MARCO MSD Focus Center and Intel Corporation.

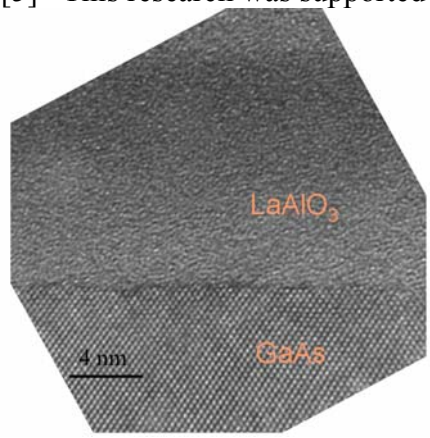

Fig.1. TEM micrograph of the interface $LaAlO_3/SiO_x/GaAs$ with a fully oxidized 1.5 nm thick *a*-Si layer after 800ºC anneal. Oxide is amorphous with clean interface.

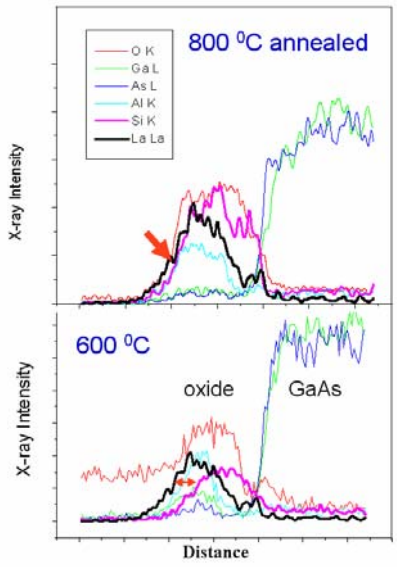

Fig.2. Cross-sectional EDX profiles of interface in Fig.1 after at 600 and 800°C annealing.

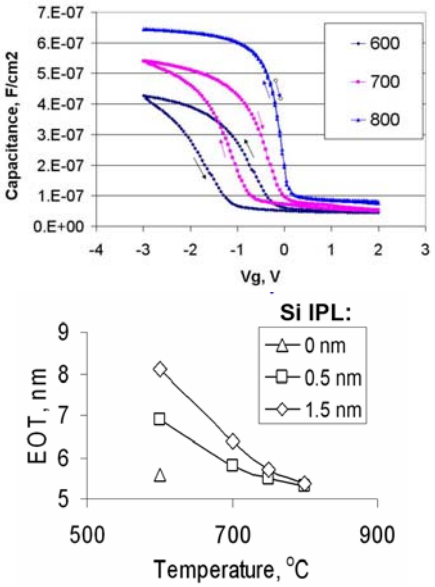

Fig. 3. Top: Effect of annealing on the *C-V* characteristics of gate stack in Fig. 1. Bottom: Contribution of the *a*-Si to EOT.

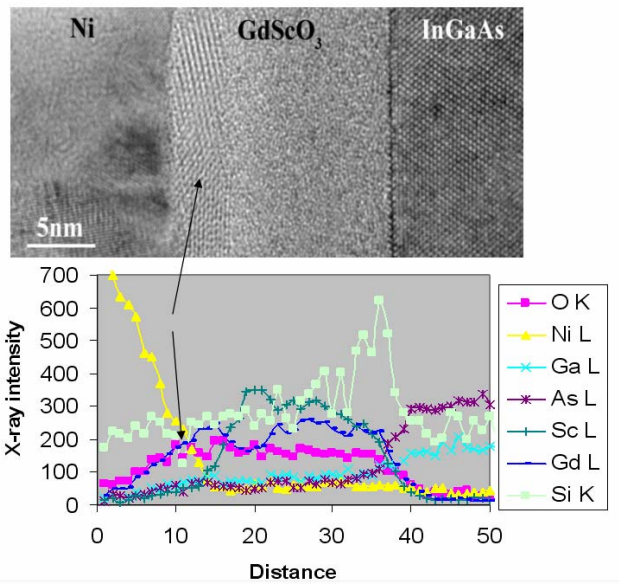

Fig.4. TEM cross-sectional micrograph and EDX profile of the $GdScO_3/SiO_x$/ InGaAs gate stack after 800 °C annealing.

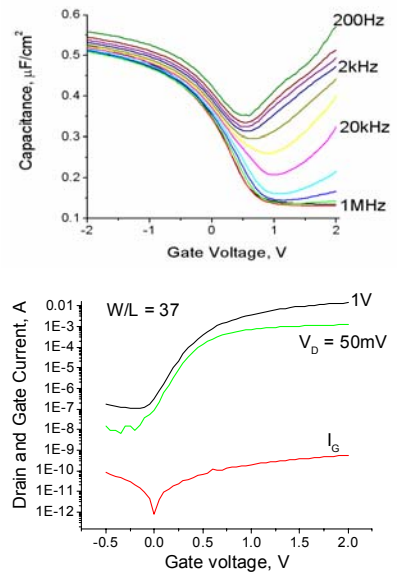

Fig. 5. Top: C-V characteristics of Ni/$GdScO_3$/ SiO_x/p-InGaAs MOS structures with Si IPL; and bottom: MOSFET input characteristics.

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