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Reducing Charging Issues in Silicon on Insulator Cross Sections Under SEM

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Silicon on insulator (SOI) wafers consist of a layer of silicon that is approximately 0.75 mm thick, an insulating silicon dioxide layer (ranging from 100nm to a few μm), topped with another silicon layer that can vary in thickness from 20 nm to a few μm. It is often beneficial to look at cross sections of silicon on insulator wafers, however under the beam of an SEM a significant charging problem arises [1] making good resolution at high magnifications difficult to accomplish. Normally, the Si layer carries away excess charge, but because the top Si layer is so thin, a charging problem persists. We aimed to utilize a conductive coating to reduce the charging problem [2]. However, as we were interested in surface features in the cross section, coating a surface other than the cross section was required. This was achieved by sputter coating a large piece of the wafer (several cm on a side) with gold and then mechanically cleaving to reveal an unobstructed cross section with a thin coating of gold on the top edge; this resulted in a significant decrease in charging and greater resolution at higher magnifications.

Samples were prepared by sputter coating gold onto the top of the sample for two minutes. This left a gold layer about 500 Å thick. The samples were then cleaved to expose the cross section, leaving a layer of gold on the surface. An uncoated and a coated sample were loaded in cross section into a JEOL 6320 FEG-SEM for comparison. Grey-scale values were compared to show that the uncoated sample would appear brighter at the SOI edge than the coated sample. An accelerating voltage of 5kV was used to collect images with a lower secondary electron detector.

Figure 1 shows the bulk silicon (or back side) of the silicon wafer in cross section. These images were used to normalize the grey values and show that the bulk silicon would be unaffected by coating on the topside. Eight bit per pixel grey values were determined in ImageJ. Under fixed conditions Si grey values away from the edge were the same (within 1%).

Figure 2 on the left shows a sample that has not been coated and is compared to the figure in the center that has been given a highly conductive coating. Plot profiles were also created from each sample and compared on the right. The blue line displays the grey values for the sample that has not been coated and the red line shows the grey values for the coated sample. The graph suggests that the oxide charging (small peaks) has been reduced, and the edge charging has been eliminated. It is interesting to note that the oxide appears darker on the sample that has been given a conductive coating than the sample that has not been treated.

Figure 3 compares, at high magnification, a sample without a conductive coating on the left and a sample with a conductive coating in the center. The image on the right shows a SOI schematic of the sample in cross section, detailing the different layers that may be visible. It is clear that there is greater resolution on the image of the coated sample while on the uncoated sample charging begins to obscure the bonding interface making focusing the image difficult. It can be concluded that coating a Silicon on Insulator sample with a highly conductive material and then cleaving it is an effective way to reduce charging in SEM cross sections.

[1] K Inai, et. al. Proc. SPIE **7140** (2008) p.0X
[2] Tony Laudate, Advanced Materials and Processes **July** (2003), p. 25.
[3] The author would like to gratefully acknowledge support from the NASA/Missouri Space Grant Consortium, Dr. P. Fraundorf for providing insight and guidance, and Dr. J. Libbert and MEMC for providing samples and funding, Dr. D. Osborn and the UMSL Center for Nanoscience MIST lab for access to equipment.

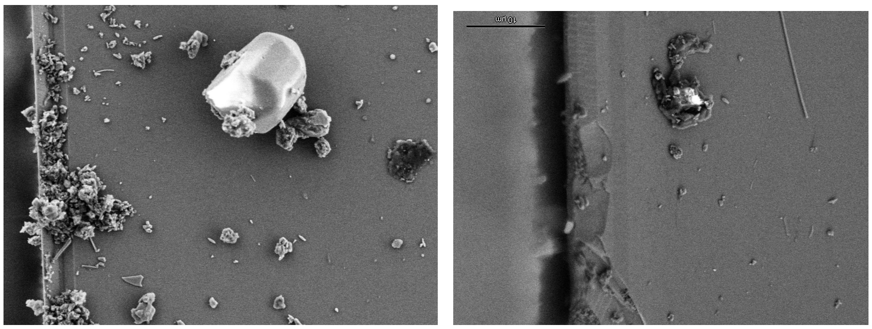

Figure 1: Bulk Si (at low magnification) grey values are unaffected by a conductive coating.

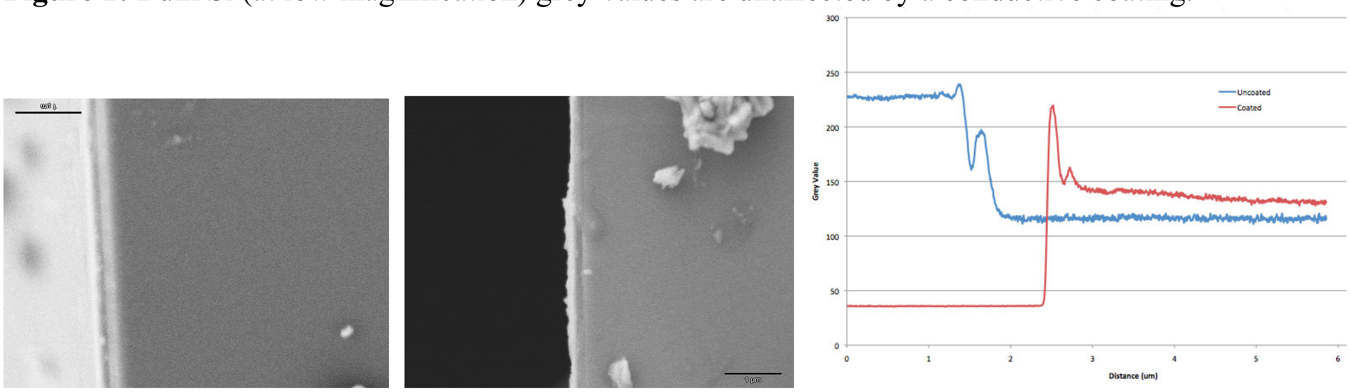

Figure 2: Comparison of uncoated and coated brightness values at low magnification.

Figure 3: Comparison of uncoated (left) and coated (center) SOI edges at high magnification. **Right:** a diagram of the coated sample at the SOI edge.

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