High-Performance Emerging Solid-State Memory Technologies

Herb Goronkin and Yang Yang, Guest Editors

Abstract

This article introduces the November 2004 issue of *MRS Bulletin* on the state of the art in solid-state memory and storage technologies. The memory business drives hundreds of billions of dollars in sales of electronic equipment per year. The incentive for continuing on the historical track outlined by Moore's law is huge, and this challenge is driving considerable investment from governments around the world as well as in private industry and universities. The problem is this: recognizing that current approaches to semiconductor-based memory are limited, what new technologies can be introduced to continue or even accelerate the pace of complexity? The articles in this issue highlight several commercially available memories, as well as memory technologies that are still in the research and development stages. What will become apparent to the reader is the huge diversity of approaches to this problem.

Keywords: *solid-state memory, storage technology.*

The world seems to have an insatiable appetite for solid-state integrated circuit memory. History shows that any memory density on the Moore's law curve is only a stepping stone to the next more complex node. Driving this escalation of complexity is the consumer's need to move from simple mathematical calculations and word processing that required only kilobits of memory to audio and movie downloads needing gigabits of memory. Near-term market demands for applications such as real-time on-demand movie viewing will require memory densities in the multi-gigabit range that can operate with communication devices in the hundreds of megabits range. But, even though the memory industry has kept pace and even facilitated challenging applications, the combination of physical barriers and cost escalation appear to be drawing Moore's law to a close, as transistors are becoming too small to function properly. Undesirable quantum effects such as electron tunneling through the gate oxide and excessive electric fields arising from small spacings preclude satisfactory operation.

Current integrated circuit memory elements are fabricated in silicon using extremely complex fabrication techniques. The exquisitely controlled interplay of chemical and physical processes that is required to fabricate hundred of millions of transistors and memory elements in a chip no larger than a couple of centimeters on a side is truly one of the wonders of the technological world. Processes that are seemingly incompatible are made to work together in a reproducible and repeatable way to produce chips of such high reliability that they can continuously operate for ten years or more in a temperature range that covers at least from 0°C to 130°C. But these processes—lithography, etching, deposition, etc.—are currently working near their limits of resolution; indeed, moving past the 30 nm node will be rather difficult. At the same time, the fundamental building blocks of integrated circuits, CMOS (complementary metal oxide semiconductor) transistors, are becoming more and more leaky as they are made smaller. Electric charge can leak through the gate oxide and from source to drain through the substrate, making the transistors unstable as memory sources.

The memory business drives hundreds of billions of dollars in sales of electronic equipment per year. Two of the major driving forces of this market are computers and wireless communication devices. The incentive for continuing on Moore's law is huge, and this challenge is prompting considerable investment from governments around the world as well as in private industry and universities. The problem is this: recognizing that current approaches to semiconductor-based memory are limited, what new technologies can be introduced to continue or even accelerate the pace of complexity?

Semiconductor memories fall into two rough categories, volatile and nonvolatile. Dynamic random-access memory (DRAM) is volatile, meaning that as charge leaks out of the memory capacitor, it must be refreshed. When memory density was relatively low, the total chip power dissipation required for refresh was also low. As memory density increased, the refresh rate of about 1–10 ms/Mbit resulted in increasingly greater energy expenditures; now the current density of DRAM, presently at 512 Mbit and moving to 1 Gbit, requires refresh energies that can dominate the power dissipation budget of the chip during standby operation.

Radically new approaches to this problem address the issues of refresh rate, memory element charge density, and process cost. Collier et al.[1] and Duan et al.[2] approach these issues by utilizing the oxidation and reduction states of specialized molecules to store ones and zeros. Collier et al. have reported on memory cells using rotaxane in which the molecular memory is the rapid reversible conductance switching of molecules attached between two electrodes.[3] Kuhr et al. (in this issue) use self-assembled porphyrin molecules that are oxidized or reduced through the application of an electric field to set the two memory states.

In spite of its increasingly higher power dissipation, DRAM is the most widely used memory in computers because it is relatively fast and inexpensive. Since DRAM is volatile, information in memory is read into the hard disk at shutdown and then re-read back into DRAM at startup. Computers that have myriad applications take a long, finger-tapping time to boot up. If DRAM were replaced with a nonvolatile memory that was at least as fast, boot-up time would be almost instantaneous because all of the information contained in active memory at shutdown would be immediately available at startup. Several types of nonvolatile memory that may be able to replace DRAM are in the research and development stage. Flash memory, a highly successful commercial nonvolatile memory, is too slow and needs higher voltages than DRAM to write information, so it is useful only in applications where those properties are acceptable to the user, for example, digital cameras and cell phones.

Because the application space for memory with unique properties is so vast, there are, seemingly, roles for many types. Computers need fast memories with high endurance that can operate for more than 1×10^{17} cycles at today's clock speeds. At the other end of the memory spectrum are games, smart cards, and PDAs that do not need such high endurance because information is entered less frequently. Researchers are, however, eager to find and develop a universal memory that can replace all current types.

In this issue of *MRS Bulletin* on High-Performance Emerging Solid-State Memory Technologies, several commercially available memories, as well as memory technologies in both research and development stages, are highlighted. Table I summarizes the distinguishing characteristics among the primary varieties. The common underlying theme of all of these articles is the further development of the respective technologies for the purpose of staying on the Moore's law complexity curve—increasing the number of memory elements—while retaining or What will become apparent to the reader is the huge diversity of approaches to this problem.

We start this issue with flash memory. Flash memory has a floating metal gate buried inside the oxide layer of a transistor, and the "0" or "1" state is determined by the charge storage status of the floating gate. Fazio presents the most recent developments in this technology that make it faster than the current generation of flash memory and can be run at a lower operating voltage.

Grynkewich et al. describe a nonvolatile memory in which current pulses change the magnetic polarization to store ones or zeros in high- or low-resistance states.[4]

Arimoto and Ishiwara describe another nonvolatile memory device in which an electrical impulse shifts the unit cell structure to change the ferroelectric polarization.[5]

Hudgens and Johnson describe yet another nonvolatile memory device using chalcogenides in which an electrical impulse changes the material phase between high- and low-resistance states.

Yang et al. introduce a thin-film organic/nanoparticle memory device in which charges stored in the nanoparticles cause the organic/polymeric layers of the device to be either in the high or low electrical conductivity states.[6]

Kuhr et al. introduce another organic memory device in which custom-designed porphyrins are oxidized or reduced by an electrical impulse to store charge in a manner analogous to a DRAM capacitor.[7]

Silva et al. describe a quantum dot memory structure in which decoupled quantum dots replace the floating gate electrode to improve the performance and broaden the application of highly scaled flash-type memories.

Whether these memories are based on semiconductors, molecules, magnetic thin films, or other materials, all have a fundamental requirement: they must reside inside a silicon CMOS chip. CMOS is the technology that the world has accepted. Multibillion-dollar factories spit out millions of chips every day to satisfy the world's appetite for industrial and consumer electronic equipment. To be successful, any new technology that is intended to sustain the evolution of electronic memory must be compatible with CMOS processing. This is not a trivial issue; in fact, integrating a new technology into CMOS is one of the most challenging of semiconductor engineering projects. CMOS processes are highly complex admixtures of high-temperature processing, 30–45 levels of photolithographic masking to form devices, interconnects, vias (vertical connectors between interconnects and devices), isolation patterns, numerous and chemically varied dry-etch processes, and other procedures. The process modules have been carefully developed so that the highest temperature occurs early in the process and the lowest temperature is last. Structures that are closest to the silicon interface experience the highest process temperatures, while interconnects, interlayer dielectrics and passivation layers, which protect the chip from the environment in the package, nearer the top of the chip structure, experience the lowest temperatures.

Considering the memory approaches described in this issue, some devices of the memory elements will reside near the bottom silicon interface while others will be near the top of the chip. What drives these locations is the capability of the memory cell to withstand high temperature. For example, flash memory elements, including quantum dot and ferroelectric cells, are located near the bottom where the memory storage volume is part of the underlying transistor structure. The flash floating gate is polysilicon, which is deposited at rather high temperatures, and the ferroelectric gate of ferroelectric random-access memory (FeRAM) is also deposited at high temperatures. Subsequent layers of vias and interconnects are deposited at lower temperatures. Magnetoresitive random-access memory (MRAM) and the molecular memories reside near the top of the chip structure because high temperatures would degrade the materials and interfaces that are critical to performance of the memory cells. These families of memory storage cells are independent of the operation and performance of the pass transistors and can therefore be located in the position most favorable to their survival in the CMOS process.

The integration of new memory cells into CMOS involves issues of material compatibility, the most serious being the potential for contamination of the silicon fab line from materials in the memory structure that are not normally used in CMOS processing. Even a minute amount of such materials as gold, nickel, iron, zinc, and many others have the potential to find their way into the silicon lattice, where they can alter the operating properties of the transistors. Recognizing this potential, process lines that integrate such divergent technologies into the same chip must find ways to protect the underlying CMOS substrate while optimizing the performance of the new memory storage cells. The solution boils down to two things: time and money.

Let's take a look at the time needed to move an idea from proof-of-concept demonstration to commercialization. The major steps along the way take the idea from proof-of-concept to feasibility demonstration, development, and finally commercialization. Experience in high-technology industries shows that the time needed to move through these phases is typically ten years. Each step closer to commercialization involves increasing numbers of workers and equipment. A new memory technology, one that introduces new materials and disrupts the established CMOS process flow, often requires dedicated process facilities that are physically separated from the main process line in order to avoid cross-contamination. It is not at all unusual for a radically new device structure that is integrated into CMOS to cost several hundred million dollars to develop and take three to five years to fully ramp up for commercialization.

DRAM, SRAM, and flash memories are the current mainstay of semiconductor-based memories. All of these have serious performance and scaling limitations, and it is only by mitigating these limitations that new memory technologies have a chance to initially augment and finally displace the current leaders. Potential performance of the new memories is only the foot-in-the-door phase. Maintaining performance at a reasonable and competitive integration cost is the real key to ultimate adoption of the technology by the memory industry. As a colleague once explained, there are three factors that drive memory: cost, cost, and cost.

Through these articles in this issue of *MRS Bulletin*, the progress and potential of solid-state CMOS-based memory devices are briefly presented. Judging by the rapid growth of digital technology in applications ranging from personal electronics to home and business applications and to novel military uses, the need for faster, cheaper, better memory devices will continue to push memory technology into an even more diverse and highly competitive business. This will lead to even more applications, many of which are waiting to be discovered. These revolutionary changes are rapidly approaching.

Table I: Comparison of Various Memory Technologies.

Acronym or Common Name	Memory Technology	Mode of Operation	Key Characteristics
DRAM	Dynamic random-access memory	Charge is stored on a capacitor that is isolated from other memory bits in the array by a transistor.	Charge leakage from the capacitor is replenished by refresh circuitry. Refresh power dissipation increases with memory density.
FeRAM, FRAM	Ferroelectric random-access memory	Two directions of remanent polarization in a ferroelectric film represent the two memory states.	A stored datum is read out by detecting the polarization reversal current of a ferroelectric capacitor or the drain current of a ferroelectric-gate field-effect transistor.
Flash memory	Floating gate memory	Charge on a floating gate modifies the threshold voltage of the underlying transistor.	High fields transfer charge to and from the floating gate of a metal oxide semiconductor device, leading to relatively slower writes compared to reads and limited write endurance.
MRAM	Magnetic tunnel junction random-access memory, magnetoresistive random-access memory	Parallel or opposite polarization of two ferromagnetic films on each side of a tunnel barrier produce high- and low-resistance paths.	The vector sum of magnetic fields generated by short-pulse currents set the relative magnetization directions. Currents through the bits are used to read the states.
ORAM	Organic random-access memory	Memory states are set due to the charge trapped in metallic nanoparticles within the organic material.	A nonvolatile memory in which organic layers are either in the high- or low-conductance modes, preset by extermal bias.
OUM^{TM}	Phase-change memory (Ovonic Unified Memory^{TM})	Two solid-state phases having different resistivities represent the two memory states.	High reliability depends on atom-positional switching reproducibility of the two phases.
QDOT	Quantum dot memory	A type of flash memory in which the floating gate is replaced by a number of randomly arranged self-assembled quantum dots.	Scales to small dimensions at which a small number of electrons in the quantum dot can produce a large voltage change in the transistor.
SRAM	Static random-access memory	A transistor and its load are latched by a second transistor and load to maintain a memory state.	A fast memory that utilizes more area than DRAM and needs constant power to maintain the memory state.
ZRAM	Molecular random-access memory	The oxidation state of porphyrin molecules produces charge states analogous to a DRAM capacitor.	Molecular memories can have high charge densities and can be scaled to nanosized dimensions.

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Following several industrial research assignments in compound semiconductors, silicon integrated circuits, optical sensors, and microwave semiconductor devices, he joined Motorola in 1977 to establish their GaAs electronics program, leading and co-developing Motorola's early versions of heterostructure transistors for low-power, low-noise wireless applications and high-efficiency power transistors for cellular telephones, including the high-efficiency heterostructure power transistor for the StarTac phone. In 1990, he won a 10-year program funded by Japan's Ministry of International Trade and Industry on quantum functional devices, which led to a practical microwave/millimeter-wave wireless communication device and circuit technology, and in 1992, he joined and staffed the 10-year Atom Technology Project. In the mid-1990s, Goronkin's lab developed a new class of low-cost, high-density DNA biochips for the analysis of genetic mutations and spun the effort into a newly formed division in 1998. His groups refocused on microfluidic technology and demonstrated cell-to-DNA biological sample preparation and analysis in a single credit-card-sized cartridge.

In 1998, Goronkin started Motorola's nanoelectronics program and contributed to national efforts that led to the creation of the National Nanotechnology Initiative. He began exploratory investigations of magnetic random-access memory (MRAM) in 1993, launched the formal program in 1995, and continued to spearhead development of MRAM at Motorola until it was transferred from the research labs to manufacturing in 2000. His labs continued to explore radical scaling of MRAM memory elements as well as new device applications of spintronic structures and materials.

Goronkin established research laboratories and collaborations in Japan, France, and Italy to further the study and development of nanoelectronics for future integrated circuits, sensors, and communication applications. Additionally, he established active collaborations with universities in the United States, Japan, and Europe to explore a diverse research agenda that balanced the long- and near-term efforts in the total network. His organization was especially successful in working with a number of universities and government laboratories in the area of spintronics.

Goronkin earned BA, MA, and PhD degrees in physics from Temple University. He is a fellow of the IEEE and a member of the American Physical Society and Sigma Xi. He has served on committees for numerous conferences and professional organizations. He holds more than 65 patents and has numerous publications. Goronkin received Motorola's Distinguished Innovator Award in 1992 and the Master Innovator Award in 1995. He was a member of Motorola's Science Advisory Board Associates and was named Senior Engineer of the Year in 1993 by the Phoenix Section of the IEEE. He was also a Motorola Dan Noble Fellow.

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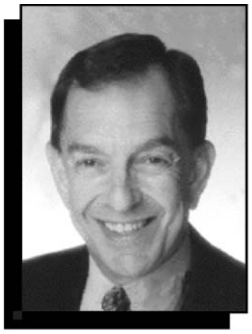
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Yang has published more than 90 refereed papers, given more than 50 invited presentations on his research work, and has filed or been granted 22 U.S. patents. He has been honored with the Outstanding Overseas Young Chinese Scientist Award from the Natural Science Foundation of China (2004), the NSF Career Award (1998), and the 3M Young Investigator Award (1998).

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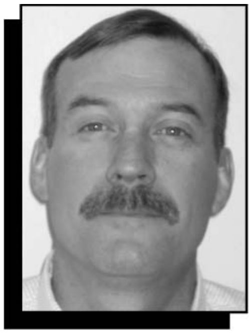

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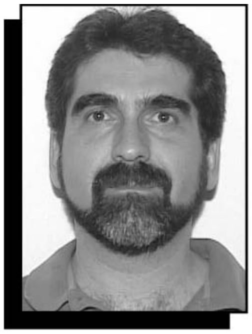

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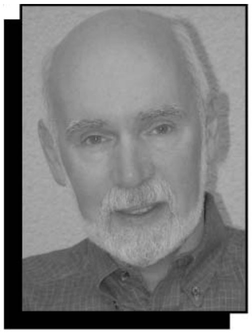

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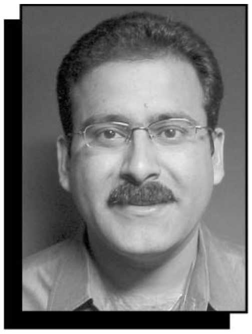

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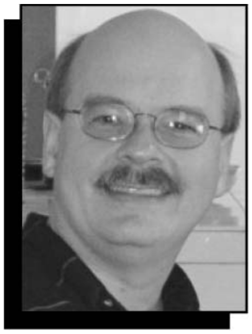

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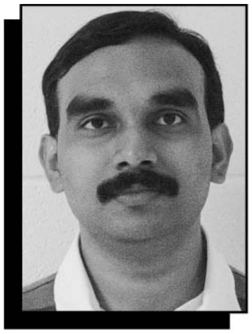

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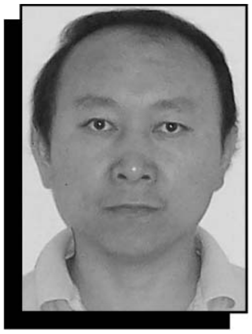

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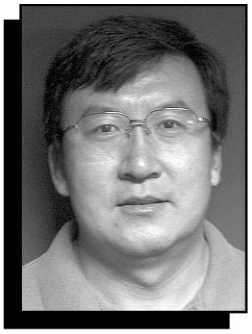

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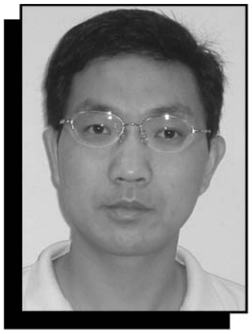

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