

Birth of a grain boundary: In situ TEM Observation of the Microstructure Evolution in HfO₂ Based Memristors

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Resistive Random Access Memory (RRAM) is one of the most promising emerging non-volatile memory concepts according to the Emerging Research Devices (Chen et al., 2013). So far reliability and device-to-device variability are still one of the key challenges regarding RRAM (Ambrogio et al., 2014). Moreover, lowering the required field to initiate resistive switching is crucial to prevent permanent device failure (Salaoru et al., 2013) and to be compatible with Complementary Metal-Oxide-Semiconductor (CMOS) (Hermes et al., 2011). To overcome these challenges, our latest approach involved the implementation of “threading” grain boundaries (GBs) in the insulator that bridge the adjacent metal electrodes resulting in a greatly improved resistive switching behavior (Petzold et al., 2019). In this study we want to investigate in detail how a “threading” GB is formed, yielding a deeper insight into the grain growth mechanism. The structural changes were monitored in situ with Transmission Electron Microscopy and Scanning Precession Electron Diffraction (SPED).

35x35µm² resistive switching devices with the structure Au/Pt/amorphous-HfO₂/TiN/Al₂O₃ were grown by Reactive Molecular Beam Epitaxy (RMBE) and sputter deposition. The forming voltages of pristine and annealed devices were measured by contacting top (Pt) and grounding bottom electrode (TiN) with a Keithley 4200 Semiconductor Characterization System (SCS) as schematically shown in Fig. 2b). From a pristine device, a cross sectional lamella was prepared by using Focused Ion Beam (FIB) and transferred onto a Micro Electrical Mechanical System (MEMS) based heating chip. During in situ heating in a JEOL ARM 200F, structural changes were monitored by TEM and SPED.

ASTAR (Nanomegas) Automated Crystal Orientation Mapping (ACOM-TEM) maps show no contrast in the HfO₂ layer for the pristine device and “threading” grain boundaries (GBs) (interconnecting Pt and TiN) in the in situ annealed device as shown in Fig. 1 a) and b), respectively. In situ monitoring grain evolution revealed that grain growth can start already at 160°C with grains growing towards each other parallel to the layer interfaces as shown in Fig. 1 c-h). Due to favorable aligned GBs in the HfO₂ insulator layer, a lowering of the required forming voltage is expected as shown by the I-V curves of a pristine and an ex situ annealed device in Fig 2a).

The “birth” of a grain boundary was in situ monitored by TEM and SPED. Grain growth started at 160°C which guarantees back-end-of-line (BEOL) compatibility. The ex situ annealed device showed reduced forming voltages in comparison to the pristine device due to the “threading” GBs interconnecting the metal electrodes. The authors acknowledge funding from the German Research Foundation (DFG) under grant No. 384682067 and the European Research Council (ERC) “Horizon 2020” Program under Grant No. 805359-FOXON.

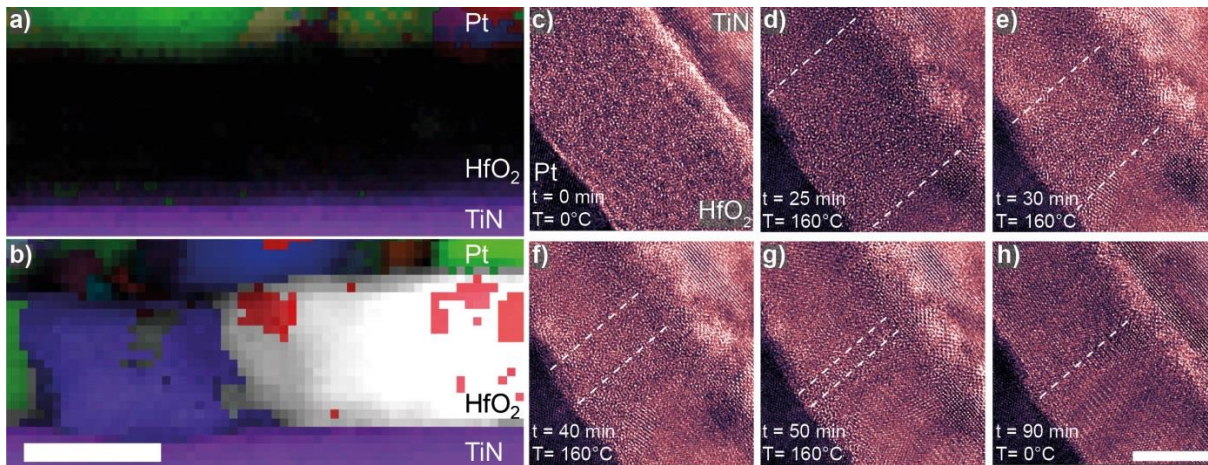


Figure 1. ACOM orientation + index mapping of a TiN/HfO₂/Pt Metal-Insulator-Metal stack shows no contrast for HfO₂ in the a) pristine device due to no preferred orientation (amorphous) and grain boundaries in HfO₂ interconnecting the metals in the b) in situ annealed device. The formation of a grain boundary was monitored in situ by using TEM c-h): at 160°C crystallization starts with two grains at the edges of the image growing towards each other perpendicular to the layer interfaces and fully merge after 90 minutes. The white hatched line is a guide to the eye to illustrate grain borders. Scale bar is 10 and 5 nm in b) and h) respectively. TEM images were colored with the split blackblue redwhite LUT.

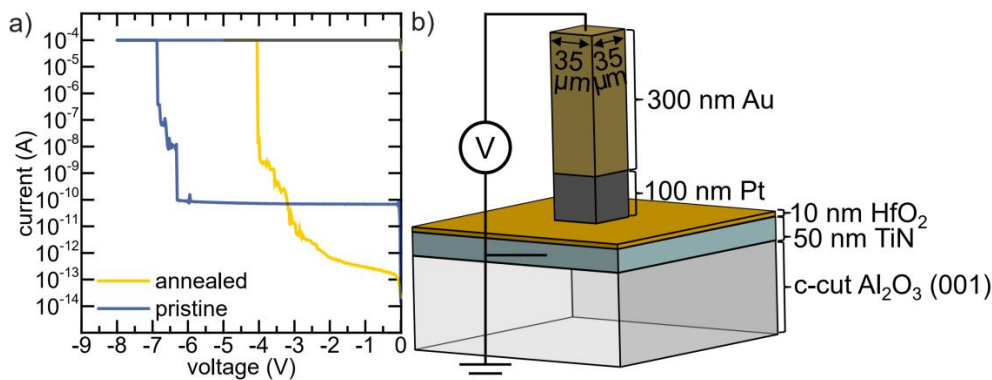


Figure 2. a) The I-V curves of initial filament formation for devices with b) stack combinations of Au/Pt/HfO₂/TiN/Al₂O₃ with a contacted top electrode and a grounded bottom electrode show a lowered forming voltage ($V_f \approx -4$ V) for the stack with annealed HfO₂ in comparison to the pristine device with amorphous HfO₂ ($V_f \approx -7$ V).

References

- AMBROGIO, S., BALATTI, S., CUBETA, A., CALDERONI, A., RAMASWAMY, N. & IELMINI, D. (2014). Statistical Fluctuations in HfO_x Resistive-Switching Memory: Part II—Random Telegraph Noise. *IEEE Transactions on Electron Devices* **61**, 2920–2927.
- CHEN, A., ZHIRNOV, V., HUTCHBY, J. & GARNER, C. M. (2013). ITRS chapter: emerging research devices. *Future Fab. Special ITRS Focus* (44).
- HERMES, C., BRUCHHAUS, R. & WASER, R. (2011). Forming-Free TiO_2 -Based Resistive Switching Devices on CMOS-Compatible W-Plugs. *IEEE Electron Device Letters* **32**, 1588–1590.
- PETZOLD, S., ZINTLER, A., EILHARDT, R., PIROS, E., KAISER, N., SHARATH, S. U., VOGEL, T., MAJOR, M., MCKENNA, K. P., MOLINA-LUNA, L. & ALFF, L. (2019). Forming-Free Grain Boundary Engineered Hafnium Oxide Resistive Random Access Memory Devices. *Advanced Electronic Materials* **5**, 1900484.
- SALAORU, I., KHIAT, A., LI, Q., BERDAN, R. & PRODROMAKIS, T. (2013). Pulse-induced resistive and capacitive switching in TiO₂ thin film devices. *Applied Physics Letters* **103**, 233513.