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e-Beam Detection of Buried Open Defects in Semiconductor Device

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e-Beam inspection is becoming popular in semiconductor high volume manufacturing (HVM) due to optical inspection's inability to detect new yield-impacting defects associated with device scaling and complex processing. e-Beam inspection uses electron optics and has the ability to electrically detect buried defects that are missed by optical inspection tools, through voltage contrast (VC) [1]. In SEM image, secondary electron yield, essentially determines the contrast among the structures at the surface of a sample. Figure 1, illustrates the dependence of secondary electron yield on the energy of incident primary beam for Mo and Pt. Furthermore, other factors like electrostatic fields and high electrical fields can modify secondary electron emission [2].

In this work e-beam inspection is used for inline detection of a buried defect in semiconductor HVM environment. The subject wafer is processed through middle of line (MOL) and then terminated post TS W-CMP step and inspected on an e-beam inspection system. The beam conditions involve a moderately high landing energy to provide energetic primary electron beam that could reach the defect location below the wafer surface and emit enough secondary electrons to provide a strong defect signal. A positive field is applied above the wafer surface to create "extracting" conditions to modify secondary electron yield by attracting secondary electrons escaping through the wafer surface towards the detector. This creates forward bias condition in the pFET and reverse bias in the nFET. Figure 2, shows nFET and pFET structures under the inspection beam conditions. A structure at the wafer surface that is grounded will have electrons flow from ground to replace those "extracted" from the surface by the electron field. A floating structure on the other hand, will not have any electrons from ground to replace the "extracted". At equilibrium, the grounded structure will have a higher "effective" secondary electron yield compared to the floating structure. The net result is the grounded structure having a brighter contrast and the floating structure a darker contrast.

Under "extracting" beam conditions an open or floating defect would appear as dark voltage contrast (DVC) and in this inspection several DVCs were detected on the wafer in nFET regions. TEM analysis is used to gain more information on the defect and determine defect mechanism. Analysis of defective sites shows a wide gap between the TS and eSD. EDX map of the TS-eSD interface reveals the presence of high levels of Florine (F). Excess process gas can react with other materials during metallization process to form compounds that prevent electrical contact between TS and eSD. This leads to device fail and can cause significant yield loss. e-Beam inspection uses this lack of conductivity between TS and eSD to flag the defective structure as the defect of interest.

The successful inline detection of this TS open defect by e-Beam inspection has been confirmed by TEM analysis. Detection provides a means for inline monitoring of defect and information gathered is used to improve process and boost yield.

References:

[1] M Soucek et al., Semiconductor International **26(8)** (2003), p. 80.
[2] L Yougui, in "Practical Electron Microscopy and Database", (GlobalSino).

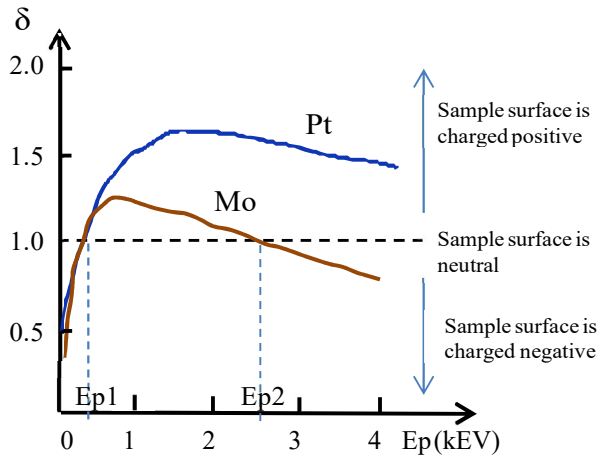

Figure 1. Dependence of secondary electron yield, δ on the energy of incident primary electrons, Ep for Pt and Mo [2]. At Ep1 and Ep2, δ = 1 and wafer surface charge is zero.

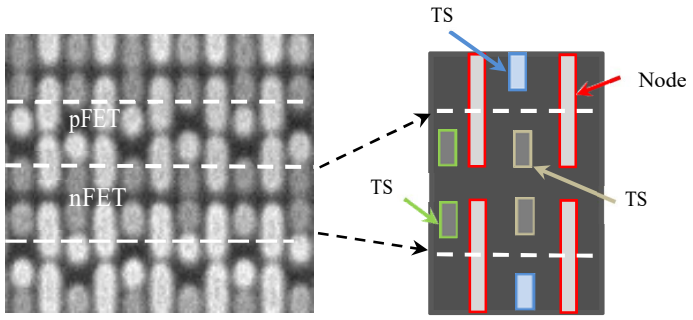

Figure 2. Live image of n/p structures on wafer surface under inspection conditions. TS structures within nFET are prone to opens.

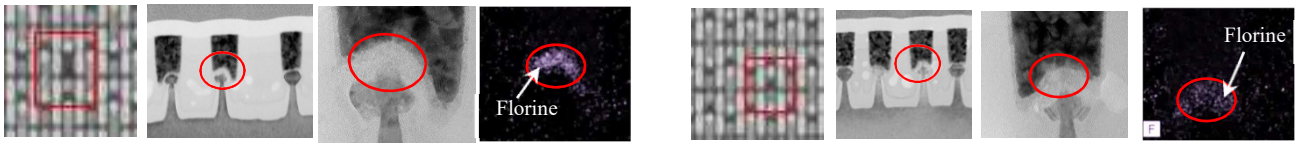

Figure 3. TEM analysis of detected TS open defects.

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