

Characterization of Defects in III-V Semiconductor Materials (InP, GaAs and InGaAs/ InP on Si) in Nano-sized Patterns by Transmission Electron Microscopy

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Recently Si-based devices have faced physical limits which are caused by the decrease of the design rule. [1] As an alternative, III-V semiconductor materials have been suggested owing to their superior mobility characteristics over Si. [2] However, in integrating III-V materials in Si-based structures, crystal defects are generated at their interfaces due to the lattice mismatch between III-V and III-V as well as III-V and Si. [3] For successful use of the III-V semiconductor as channel materials in Si based structures, such issues of defect formation should be resolved.

In this investigation, we studied the defect generation in the case of III-V compounds of InP, GaAs, and InGaAs/ InP on Si substrate with nano-sized trench structures. Also, few additional blanket samples prepared on various Si substrates was analyzed to compare with effects of patterning by transmission electron microscopy. The TEM samples were prepared by Focused Ion Beam because the pattern size of region of interesting was too narrow, moreover, a specific plane view specimen was required of three dimensional analysis. III-V compounds such as InP and GaAs were grown in the trench patterns by metalorganic chemical vapor deposition.

The pattern size of samples split 30 nm, 60 nm, and 90 nm to identify the size effect. In 30 nm and 60 nm patterns, GaAs showed stacking fault defects (SF) and twin boundary (TW) defects evenly, although in 90 nm pattern, threading dislocation (TD) defects appeared similarly with blanket samples of parallel bottom shape and large growth area. In the InP sample, the 90 nm pattern sample had threading dislocation defects like as the 90 nm GaAs sample. However, in the 30 nm and 60 nm patterns, stacking fault was major defect and twin boundary was minor defect on the contrary to expectation.

Plain-view (z axis) samples as well as cross-sectional TEM samples were made to confirm that the defects grew along the directions parallel and perpendicular to the trenches. Plan view images show defects of different angles of stacking faults and twin boundaries. Such defects are formed mostly along the (111) plane and observed along the directions parallel or vertical to the [110]. The various angles of the defects appeared in the TEM images are due to the structural formation of the multiple twin boundaries or pyramidal defects. Multiple twin boundaries are formed by the several twin defects along (111) twin boundaries. [4]

The effects of (111) and (100) orientation and surface tilting (0° and 6° tilting) substrate were examined, too. The major defects are stacking faults or twin boundaries depending on the deposited III-V films in the trench patterns on Si. The defect characteristic of GaAs grown on different type of Si such as (100), 6° tilted (100), and (111) substrates. The threading dislocation was detected in the blanket sample, and each sample had a different defect condition. The 6° tilted (100) and (111) substrate

samples had more threading dislocation defects than the (100) substrate sample.

In summary, we have investigated the formation of defects in the different pattern sizes and substrates. We confirmed the structures of the defects in three dimensional view using cross sectional as well as plan view TEM analysis.

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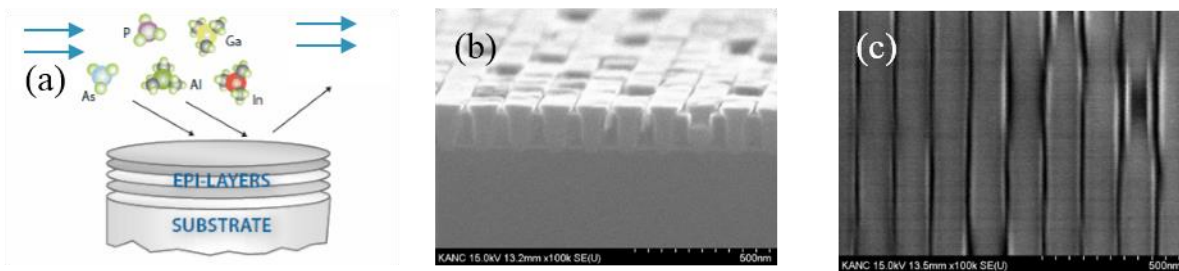


Figure 1. Shows (a) III-V compound process, (b) results of SEM cross section image and (c) Top view image.

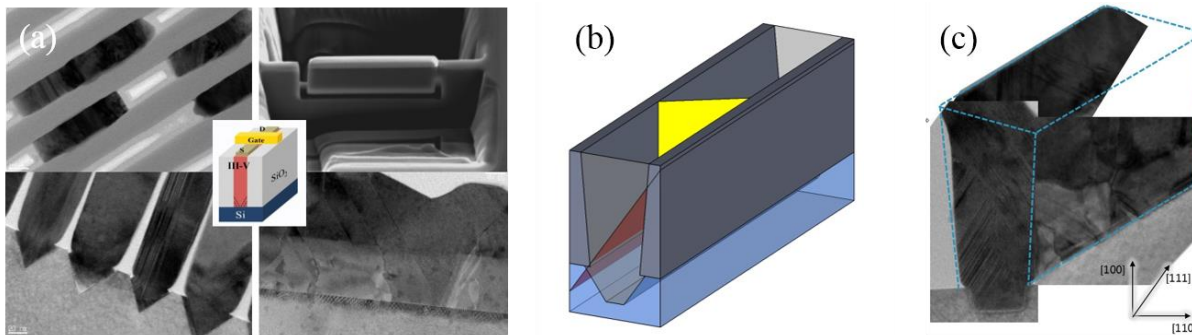


Figure 2. Shows (a) X,Y, and Z axis TEM images. (b) 3D reconstruction of [-111] twin boundary. (c) TEM 3D images of X, Y axis and plane view.

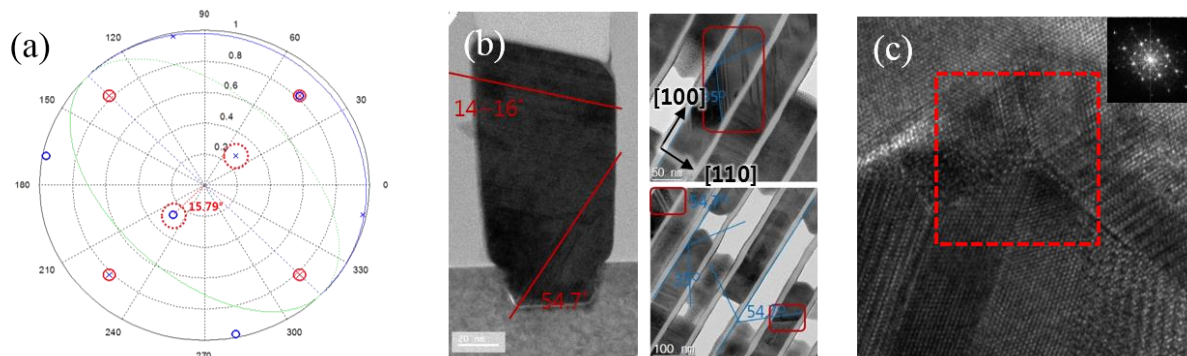


Figure 3. shows (a) Stereograph of 2nd twin boundary. (b) Defect analysis of TEM images (c) The HR-TEM and SACD image of 5 folds twin boundary.