

## Advanced Characterization of Emerging Semiconductor Devices Using Low Energy, Broad Ion Beam Argon Milling

P. Nowakowski<sup>1</sup>, J. Sagar<sup>2</sup>, M.L. Ray<sup>1</sup> and P.E. Fischione<sup>1</sup>

<sup>1</sup> E.A. Fischione Instruments, Inc., 9003 Corporate Circle, Export, PA, USA

<sup>2</sup> Oxford Instruments NanoAnalysis, Halifax Road, High Wycombe, Bucks, UK

The semiconductor industry relies upon failure analysis (FA) to determine the root cause of a defective device; it enables failure identification and characterization, as well as provides feedback for product and process improvement. Many failure analysis techniques, both nondestructive and destructive, have been developed in the past five decades. Nondestructive techniques include electrical measurement and testing, infrared and X-ray examination, and optical or electron microscopy evaluation. Destructive techniques include chemical etching, mechanical polishing, plasma etching, and delayering.

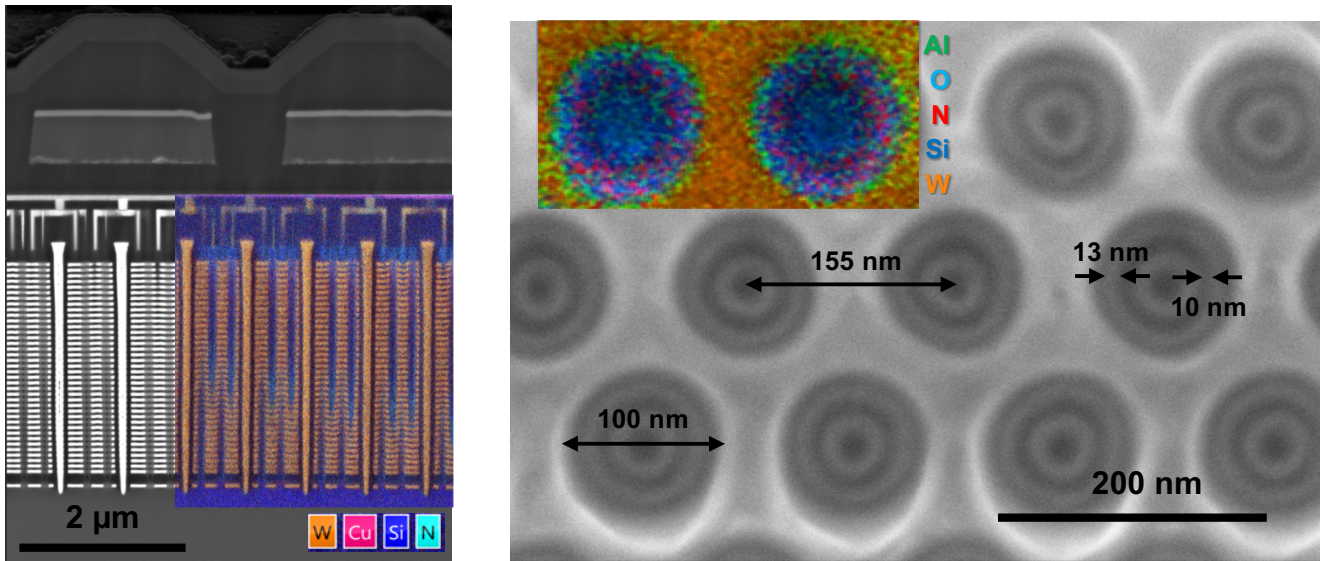
Delayering is a popular choice because it allows top-down, whole chip characterization. The primary challenges presented by a vertical stack are looking through many dissimilar layers and attempting to investigate different layers simultaneously [1]. Top-down delayering using conventional mechanical preparation techniques is a difficult and uncontrolled process that does not allow targeting of a specific depth or layer [1, 2]. Gallium and xenon focus ion beam (FIB) techniques have also been employed [1, 3, 4] – both of which present limitations that include a relatively small delayering area: about 20 x 20 µm for Ga FIB [1] and about 100 x 100 µm for Xe FIB [4, 5]. This size limitation makes it impossible to prepare a large slope area with the goal of exposing all the layers simultaneously.

Cross-section sample configurations are also widely used in microelectronics industry; this is often done by cleaving and mechanically polishing or, alternatively, FIB processing. As in the case of delayering, these techniques have similar limitations. Therefore, there is a need for a precise, fast, and relatively simple delayering and cross-sectioning process.

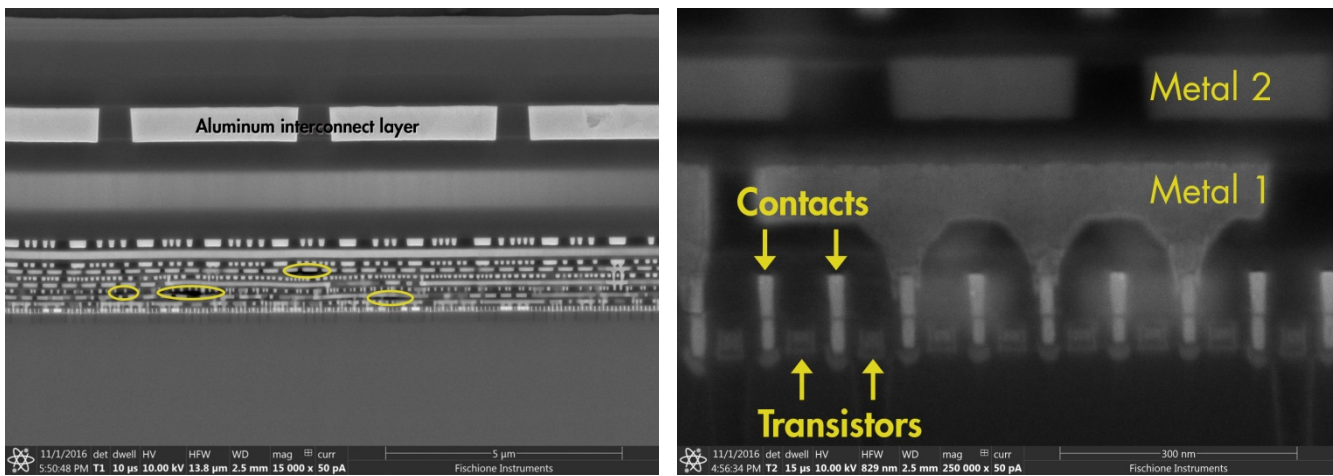
Broad ion beam argon milling has an advantage in that it allows material removal from larger areas. This new technique also allows large slope area preparation, as well as a precise and controlled delayering process. The objective of this paper is to present a new development in semiconductor device delayering for failure analysis using low energy, broad ion beam argon milling using Fischione Instruments' SEM Mill and WaferMill™ ion beam delayering solution [6]. The results were obtained using two commercially available devices: Samsung V-NAND 3D memory (Figure 1) and Qualcomm "Snapdragon" processor (Figure 2).

### References:

- [1] DD Wang *et al*, AIP Adv. **5** (2015) 127101.
- [2] AC Bonora, Solid State Technol. **20** (1977), p. 55.
- [3] HH Yap *et al*, Microelectron. Reliab. **55** (2015), p. 1611.
- [4] JV Obona *et al*, Microsc. Microanal. **22** (2016), p. 56.
- [5] R Alvis *et al*, Conf. Proc. Int. Symp. Test. Failure Anal. (2015) p. 393.
- [6] P Nowakowski, In press.



**Figure 1.** Samsung V-NAND 3D memory cross-section (left) and memory channels from delayering process (right). Scanning electron microscope image (SEM) and energy dispersive spectroscopy (EDS) mapping acquired at 3 keV.



**Figure 2.** Cross section of a Qualcomm Snapdragon processor (left). The circled areas indicate defects. The same processor shown at greater magnification (right).