

## Is It Feasible To Routinely Check The Dopant Profiling Via Off-Axis Electron Holography For An IC Failure Analysis Laboratory?

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Transmission electron holography is nearly a full developed technique at current stage, but the sample preparation is still the bottleneck for the widely use of electron holography to study the dopant profiling in the IC industry [1,2]. Focus ion beam offers us the ability to prepare the site-specific, reproducible, and constant thickness TEM specimens. For the throughput consideration, we proposed the so-called lift-out method for the dopant profiling sample preparation. First, milling of trenches on both sides at the region of interest from a full wafer. When the membrane is thinned down to about 200-300 nm thick, we cut the sample free. Then, plucking the sample out uses a glass needle. After placing the plucked sample onto the holey-Carbon support grid, we truncate the top Pt-deposition layer in order to expose the transistor to a vacuum area. The Pt-deposition layer is used to protect the specimen and increase the image contrast during milling. Fig. 1 shows a typical sample prepared by the method described above. Specimen preparation requirements for dopant profiling include: a vacuum area near the region of interest; constant sample thickness ranges from 200 to 300 nm; no curtaining or wedged-shape effects; no specimen charging. In this research, we used the FEI automatic TEM preparation wizard to meet the above sample preparation requirements. Angular cut or deep milling of trenches could be used to minimize the curtaining effects and the Carbon coating could mitigate the specimen charging. The whole process for the dopant profiling sample preparation will take about 1.5 hours.

A FEI Dual-Beam 235 and a Tecnai F30 with Lorentz lens operated at 250kV were used to prepare the sample and record the electron holograms. Using the Lorentz lens as the imaging lens offers us much wider holographic field of view ranging from 0.4 to 1.5  $\mu\text{m}$ . Electron holography enables us to recover the electron phase from the specimen's exit-face wave function. The principal contributions to the reconstructed phase image of the dopant profiling include Mean Inner Potential, electric field (p-n junction), and the sample thickness. Fig. 2 shows a bright-field TEM image of PMOS transistors. Except the diffraction contrast, there is no other contrast around the dopant area. A typical hologram of the PMOS transistor with the field of view of about 450 nm is shown in Fig. 3. Taking a reference hologram is also necessary to remove the artifacts from the imaging system for each hologram. The holographic fringe contrast of the recorded hologram is  $\sim 25\%$ . Fig. 4 shows the reconstructed phase images of the PMOS transistor. A thickness map derived from the reconstructed amplitude image indicated  $\sim 250\text{nm}$  constant sample thickness around the dopant area without seeing any curtaining effects. The contrast around the dopant area roughly matches with the Boron dopant profiling. In summary, it is feasible to routinely check dopant profiling via the electron holography for an IC failure analysis laboratory since the sample preparation using the FIB lift-out method is reliable and reproducible.

## References:

- [1] W.-D. Rau et al., Phys. Rev. Lett. **82**, 2614 (1999).  
 [2] M.R. McCartney et al., Appl. Phys. Lett. **80**, 3213 (2002).

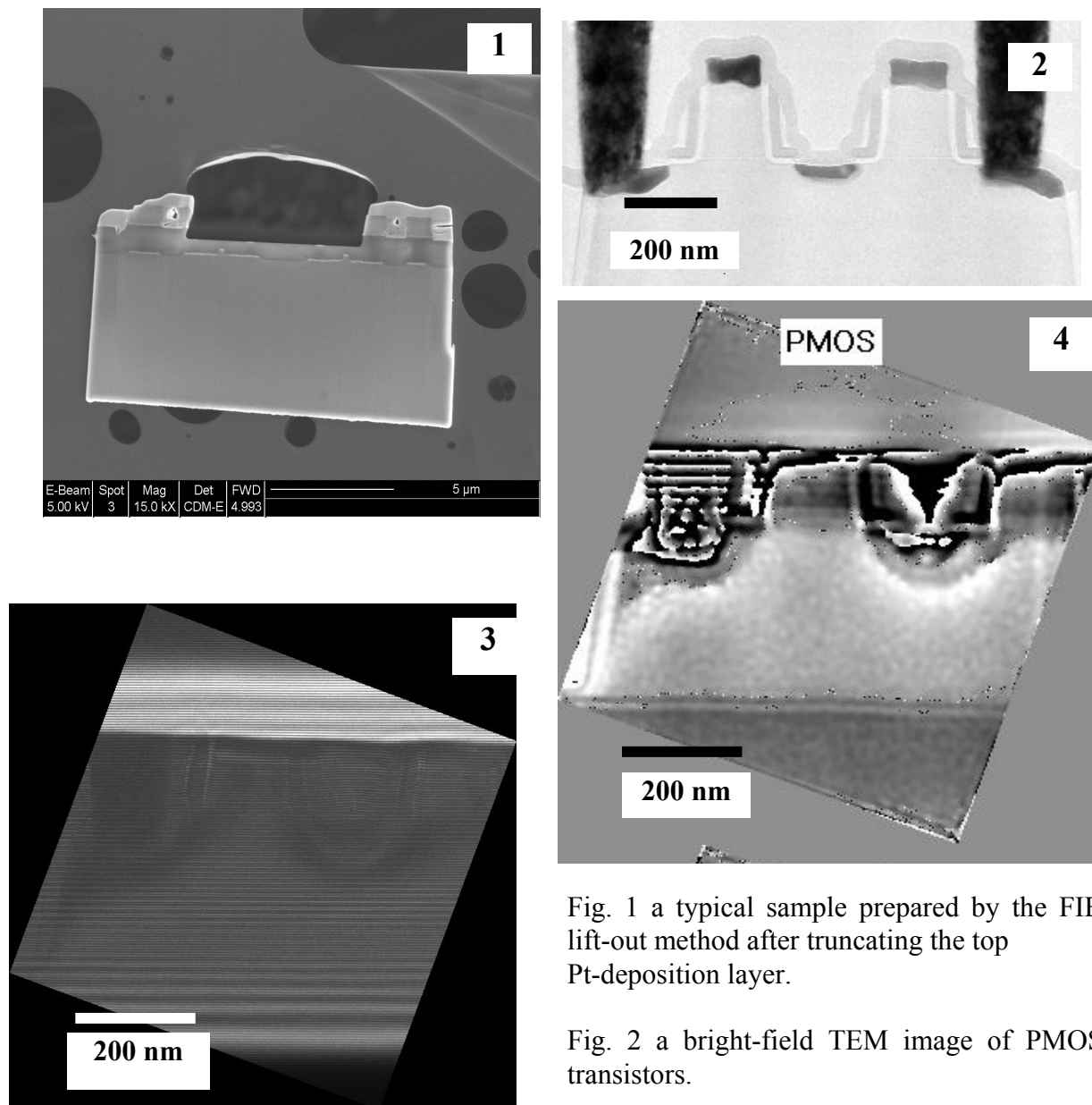


Fig. 1 a typical sample prepared by the FIB lift-out method after truncating the top Pt-deposition layer.

Fig. 2 a bright-field TEM image of PMOS transistors.

Fig. 3 a hologram of the PMOS transistor.

Fig. 4 the reconstructed phase images of the PMOS transistor.