

## Material engineering for silicon tunnel field-effect transistors: isoelectronic trap technology

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### Abstract

The tunnel field-effect transistor (TFET) is one of the candidates replacing conventional metal–oxide–semiconductor field-effect transistors to realize low-power-consumption large-scale integration (LSI). The most significant issue in the practical application of TFETs concerns their low tunneling current. Si is an indirect-gap material having a low band-to-band tunneling probability and is not favored for the channel. However, a new technology to enhance tunneling current in Si-TFETs utilizing the isoelectronic trap (IET) technology was recently proposed. IET technology provides a new approach to realize low-power-consumption LSIs with TFETs. The present paper reviews the state-of-the-art research and future prospects of Si-TFETs with IET technology.

### Introduction

The performance improvement of large-scale integration (LSI) has progressed owing to the miniaturization of transistors. The degree of integration has increased following Moore's law, which predicted that the number of components in LSI would double every 2 years.<sup>[1,2]</sup> This prediction has surprisingly come true since—the semiconductor industry has made constant efforts to continue satisfying the law. The increase in the number of transistors has been directly linked to the growth of computing performance, and such continuous improvement of computing performance has been realized over the last 70 years.

Koomey et al. examined the strong correlation between computing performance and power efficiency of computation.<sup>[3]</sup> Their work showed that the improvement of power efficiency is essential for the improvement of computing performance. From the perspective of electronic devices, the improvement of power consumption of transistors paved the way to increase the available number of transistors with a limited power supply, which resulted in the successful improvement of computing performance. In other words, low-power consumption is the essence of transistor miniaturization. This has enabled us to realize outstanding applications such as notebook personal computers, smartphones, tablets, and so on.

Dennard scaling guided the miniaturization of metal–oxide–semiconductor field-effect transistors (MOSFETs), which are

the building blocks of contemporary LSIs.<sup>[4]</sup> Dennard scaling provides guidelines to reduce the power consumption of MOSFETs with device-size miniaturization. However, Dennard scaling is not valid any longer for the state-of-the-art MOSFETs, because of short-channel effects.<sup>[5]</sup> However, the semiconductor industry has achieved both miniaturization and the reduction of power consumption after the era of Dennard scaling, in which the key technologies were finFETs,<sup>[6]</sup> SOI-FETs,<sup>[7]</sup> and high-*k* technology<sup>[8]</sup> to enhance electrostatic gate control. In the current situation, the scaling law seems to have been prolonged, but some new technologies have realized miniaturization and low-power consumption together.

Now, we are at the last stage of miniaturization. However, the enhancement of computing performance is still a demand because of new applications such as machine learning and artificial intelligence. In this situation, the reduction of power consumption must be continued even if miniaturization has been completed.

An approach to reduce the power consumption without miniaturization is the use of steep slope devices (SSDs) as new building blocks for LSIs instead of MOSFETs. SSDs can realize much steeper switching from the OFF to ON state, resulting in decreasing voltage for switching. MOSFETs have a physical limit that the sub-threshold swing (SS) cannot be  $< 60$  mV/decade at 300 K.<sup>[9]</sup> SSDs can operate with an SS  $< 60$  mV/decade; thus, they can operate at a lower voltage compared with the operating voltage of MOSFETs, resulting in low-power consumption. Some existing candidates for SSDs are tunnel field-effect transistors (TFETs),<sup>[10]</sup> negative capacitance FETs,<sup>[11]</sup> and threshold switches.<sup>[12]</sup>

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This paper concerns TFETs, which are a type of gated p–i–n diodes and have MOSFET-like structures in which the source and drain show different types of conduction. In TFETs, the tunnel barrier is a pn junction at the source side edge of the gate. The gate electrostatic control regulates tunneling current flowing through the barrier by changing the thickness of the pn junction, which enables TFETs to realize steeper switching compared with that of MOSFETs. Stuetzer’s and Shockley’s experiments have formed the foundation of TFET-like devices.<sup>[13,14]</sup> Modern TFETs having the MOS structure were proposed by Quinn et al.<sup>[15]</sup> and independently demonstrated by Baba.<sup>[16]</sup> Appenzeller et al. first demonstrated sub-60 mV/decade operation using a carbon-nanotube TFET.<sup>[17]</sup> Choi et al. first demonstrated sub-60 mV/decade operation in Si-TFETs.<sup>[18]</sup> Since then, many research groups have reported sub-60 mV/decade operation of Si-TFETs.<sup>[19–24]</sup>

The low ON current ( $I_{ON}$ ) is the most significant issue in TFET research. The  $I_{ON}$  of TFETs is still not sufficient for practically fast circuit operation. TFETs inherently have a high-resistance tunneling barrier. As the tunneling current is essentially related to material science, many TFETs with new materials, including not only Ge or III–V materials<sup>[25]</sup> but also two-dimensional semiconductors,<sup>[26]</sup> have been reported. Recently, a material engineering technique to enhance tunneling current in Si has been proposed, which utilizes isoelectronic traps (IETs),<sup>[27,28]</sup> Experimental demonstrations of the current enhancement and improvement of circuit performance have been reported,<sup>[27,29]</sup> in which IET-assisted tunneling (IETT) is utilized instead of conventional band-to-band tunneling (BTBT).

This paper reviews the IET technology to enhance  $I_{ON}$  in Si-TFETs. General issues concerning TFETs have been reviewed in.<sup>[10,30]</sup> First, we present an overview of the state-of-the-art TFET research. Then, we examine the IET technology for Si-TFETs.

## Overview of state-of-the-art TFET research

### Guidelines to enhance BTBT

Before starting to discuss IET technology, we briefly discuss the conventional guidelines to improve TFET performance, aiming to summarize the background of the IET technology.

BTBT through a pn junction is categorized as Esaki tunneling under a forward bias or as Zener tunneling under a reverse bias. TFETs utilize Zener tunneling [Fig. 1(a)]. We begin with the equation of tunneling current flowing through a junction sandwiched between two electrodes<sup>[31]</sup>:

$$I \propto \int [f_1(E) - f_2(E)] |M|^2 D_1(E) D_2(E) dE, \quad (1)$$

where  $f(E)$  is a Fermi function,  $M$  is a transfer matrix element for transition, and  $D(E)$  is a density-of-state (DOS) function. Tunneling is a transition between two states. Thus,  $M$  can be

expressed following Fermi’s golden rule as

$$|M|^2 \propto |\langle \psi_2 | -Fx | \psi_1 \rangle|^2, \quad (2)$$

where  $\psi$  is a wave function and the perturbative transition Hamiltonian is  $-Fx$ , in which  $F$  is the strength of the electric field at the junction, and  $x$  is the electron coordinate along the tunneling direction. In the case of BTBT through a pn junction,  $\psi_1$  is the state of valence band maximum (VBM), and  $\psi_2$  is that of conduction band minimum (CBM).

Equation (2) provides the first guideline to enhance tunneling current in TFETs: we should aim to increase the value of the integral on the right-hand side of the equation. Among conventional semiconductor materials used in electronic devices, which have crystal structures such as diamond, zincblende, and wurtzite, direct-band gap semiconductors, such as InGaAs, have a p-like VBM state and an s-like CBM state. Here the integral on the right-hand side of Eq. (2) has a significant value. In contrast, indirect-gap semiconductors, such as Si, have p-like CBM and VBM states, because of which the integral on the right-hand side has an insignificant value [Fig. 1(b)]. In indirect-gap semiconductors, as in the case of luminescence, phonon-assisted indirect tunneling occurs; however, its transition probability is lower than that of direct tunneling. This situation can be understood as the wave-number conservation rule. However, the indirect Ge case, in which direct tunneling occurs because the direct gap energy is close to the indirect gap energy, is complicated.<sup>[32]</sup> The direct/indirect tunneling current can be experimentally distinguished by temperature-dependent electric measurements.<sup>[28]</sup>

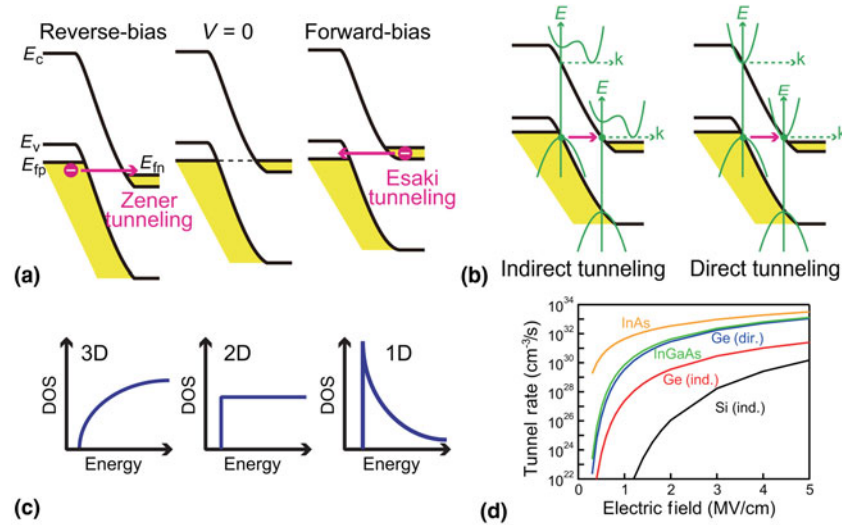
The second guideline is related to DOS, as expressed in Eq. (1). A higher DOS results in a higher tunneling current. Furthermore, the DOS depends on the dimensionality of a system, which affects  $SS$  [Fig. 1(c)]. For example, the step function of the DOS in two-dimensional (2D) systems leads us to expect steeper switching than in the corresponding three-dimensional (3D) case.<sup>[33–35]</sup> This is also valid in one-dimensional (1D) systems. Thus, low-dimensional systems like 2D semiconductors or nanowires have an advantage in terms of  $SS$  in addition to electrostatic control, as expected in MOSFETs.

Kane derived a familiar equation for Zener’s BTBT,<sup>[36]</sup> which yields the third guideline. The equation for tunneling rate  $G$ , which is proportional to  $I$ , is expressed as<sup>[32,36]</sup>

$$G = AF^P \exp\left(-\frac{B}{F}\right), \quad (3)$$

where  $A$  and  $B$  are Kane tunneling parameters, and  $P$  is 2 and 2.5 for direct and indirect BTBT, respectively. In the case of direct BTBT, the Kane tunneling parameters are

$$A = \frac{gm_v^{1/2} q^2}{\pi h^2 E_g^{1/2}}, \quad (4)$$



**Figure 1.** (a) Schematic band diagrams for a pn diode. (b) Schematic views of indirect and direct processes for Zener tunneling. The  $E$ - $k$  relationship is superimposed on band diagrams. (c) Density of states for free electrons in 3D, 2D, and 1D systems. (d) Tunneling rates for typical semiconductors calculated with Eqs. (3)–(5).

$$B = \frac{\pi^2 m_r^{1/2} E_g^{3/2}}{qh}, \quad (5)$$

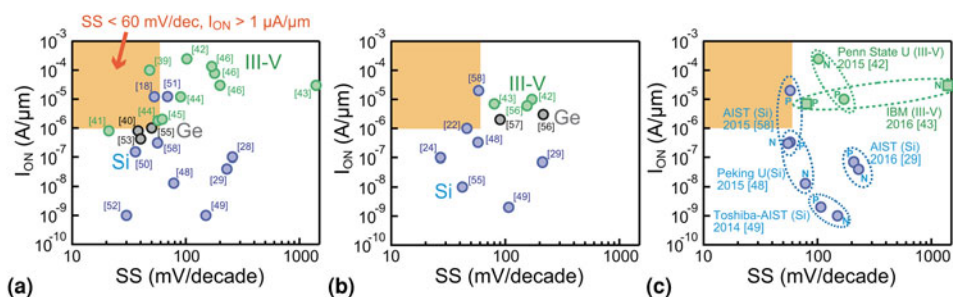
where  $g$  is a degeneracy factor,  $m_r$  is the tunnel mass ( $1/m_r = 1/m_c + 1/m_v$ , where  $m_c$  and  $m_v$  are the effective masses for conduction and valence bands, respectively), and  $E_g$  is the band gap energy. According to Eqs. (3) and (5), a smaller  $B$  results in a higher tunneling current. Then, according to Eq. (5), we can expect a higher tunneling current with smaller  $E_g$  and  $m_r$ . Qualitatively speaking,  $m_c$  is proportional to  $E_g^{3/2}$ ; therefore, we can choose materials having both a small  $E_g$  and small  $m_r$ . However, materials with a smaller effective mass have a smaller DOS.<sup>[38]</sup> Because of this trade-off relationship, a balance between  $E_g$  and  $m_r$ , as expressed in Eq. (4), is required. Figure 1(d) shows a plot of  $G$  versus  $F$  calculated using Eqs. (3)–(5) for typical semiconductor materials. It is noted that the OFF current in TFETs increases with decreasing  $E_g$  because of the lower tunneling barrier, although here we discuss  $I_{ON}$  and  $SS$  only.

As discussed above, the guidelines to obtain a higher tunneling current are the utilization of direct-gap semiconductors with lower  $E_g$  (so as to not increase the OFF current) and low-dimensional device structures.

### Device demonstrations

To our knowledge, the best performance thus far was reported in Lund University for an N-type nanowire TFET, in which an InAs/GaAsSb heterojunction was utilized.<sup>[36]</sup> The device exhibited  $I_{ON} = 10 \mu\text{A}/\mu\text{m}$  and  $SS = 48 \text{ mV}/\text{decade}$  at  $V_{DS} = 0.3 \text{ V}$ . The device follows the guidelines discussed in the previous section.

Figure 2(a) shows a benchmark for experimentally demonstrated N-type TFETs. III-V TFETs exhibit higher  $I_{ON}$  values. The benchmark follows the guidelines discussed in the previous section. For Ge-TFETs, which can utilize direct tunneling, the highest performance reported thus far was achieved in Tokyo University.<sup>[37]</sup> The highest  $SS$  of 21 mV/decade was achieved in Hokkaido University with InAs/Si heterojunction



**Figure 2.** Benchmark plots for (a) N-type and (b) P-type TFETs. (c) A plot for a limited number of samples realizing integration.

nanowire TFETs.<sup>[38]</sup> For Si-TFETs, two devices showing better performance have been reported<sup>[18,51]</sup>; however, because these two devices were operated with a relatively high operation voltage, we cannot compare them with the devices shown in this benchmark.

Some discussions are required on P-type TFETs. Figure 2(b) shows a benchmark for P-type TFETs. Surprisingly, Si-TFETs, which are expected to show poor performance because of indirect tunneling, exhibits better performance than III–V and Ge TFETs. This is probably because it is difficult to fabricate the source–channel junction for P-type TFETs with III–V materials or Ge, for which the source is n-type and the channel is p-type. At present, we do not have a solution for this problem, but some articles discussed the feasibility of realizing P-type TFETs with these materials.<sup>[56]</sup>

Recently, some papers reported the experimental demonstration of TFET integration. Six papers reported the fabrication of both types of TFETs on the same wafer. A benchmark limited to these six papers is shown in Fig. 2(c). Of these, two papers utilized III–V TFETs,<sup>[42,43]</sup> and the other four utilized Si-TFETs.<sup>[29,48,49,58]</sup> Si-TFETs show good performance owing to the ease of integration. The guidelines for TFET development are as discussed in the previous section; however, there remain difficulties in satisfying all the guidelines.

### Isoelectronic trap (IET) technology Concept

For taking advantage of the ease of integration of Si-TFETs, we aim to enhance  $I_{ON}$  in Si-TFETs sufficiently for practical application. However, the BTBT rate in Si-TFETs is low in principle. A new idea to enhance  $I_{ON}$  in Si-TFETs is to utilize a tunneling path different from BTBT, and Mori et al. proposed the use of IET technology.<sup>[27,28]</sup> The proposal is to produce an intermediate isolated state in the pn junction and utilize the tunneling current mediated by the state [Fig. 3(a)]. The intermediate state acts as a “stepping stone” for electrons tunneling from the valence to conduction bands. Thus, we can realize a tunneling path different from BTBT. In this idea, the key point is the concentration of the intermediate state. The concentration should be sufficiently low such that the intermediate state is

isolated and does not form a band. In this situation, the intermediate state is not selective in terms of wave numbers, like atoms. In other words, the intermediate state can take any wave number because of the uncertainty principle. Following this scenario, we can aim to relax the  $k$ -conservation rule in indirect-gap semiconductors and realize pseudo-direct tunneling to obtain a higher tunneling rate. Here isoelectronic impurities (IEIs) are chosen to form the intermediate state. Specifically, the Al–N pair is chosen, as discussed later.

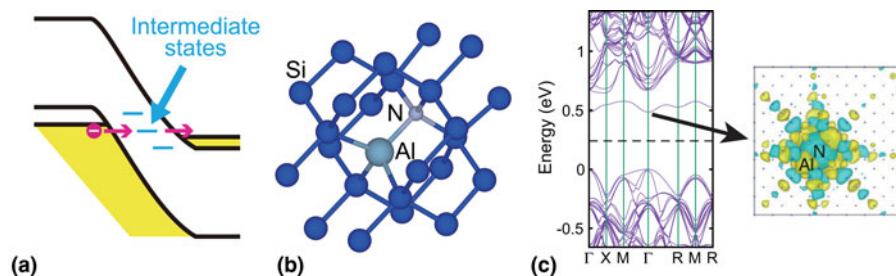
### Isoelectronic impurities

There is a long history of research on IEIs, which have been mentioned in papers published in the 1960s. IEIs are also called “isovalent electron impurities” because the impurities are isovalent with the host material and do not produce carriers. In the simplest substitutional view, for Si, other group-IV elements such as C, Ge, and Sn can be IEIs. The impurity pairs following the octet rule, such as III–V and II–VI pairs, are also IEIs if they do not produce dangling bonds. The definition as not producing carriers is notably wide, but the IEIs of interest form states in the band gap of host materials and produce unique physical phenomena such as luminescence. The mechanisms for the formation of states by IEIs have been discussed previously.<sup>[59]</sup> There are two scenarios: one is that the core charge, different from that of the host material, provides strong short-range potential perturbation, while the other is that the atom-size difference between the IEIs produces local strains resulting in potential perturbation in the host material.

Thus far, the most successful application of IEIs has been green light-emitting diodes (LEDs) realized using GaP:N before the InGaN era. GaP is an indirect-gap host material.<sup>[60]</sup> The IEI in this application is N, which forms N–N pairs in the host GaP and realizes strong pseudo-direct luminescence at room temperature. Specifically, the luminescence originates from the exciton emission bound to the IET.

### Isoelectronic impurities in silicon

The IEIs in Si have also been studied with the motivation to realize LEDs. Unfortunately, the binding energy of excitons bound to IET states is not sufficient for emission at room



**Figure 3.** (a) Schematic representation showing the idea of using intermediate states for tunneling through a pn junction. (b) Schematic atomic configuration of an Al–N pair in a host Si crystal. (c) Calculated band diagram of Si with an Al–N pair. The Al–N pair provides a discrete state in the band gap. The wave function of the discrete state at the  $\Gamma$  point is also shown.

temperature, because of which its practical application has not been realized yet. The situation of IETs in Si is slightly complicated. The substitutional C, Ge, and Sn—the previously called “simple” IEIs—do not exhibit the exciton emission bound to the IETs. It is supposed that these IEIs do not yield the important states in the band gap. The IET emissions were observed with single-atom IEIs, which are In,<sup>[61]</sup> Be,<sup>[62]</sup> Cu,<sup>[63]</sup> S,<sup>[64]</sup> Se,<sup>[65]</sup> and Zn,<sup>[66]</sup> and an atom-pair IEI, which is Al–N.<sup>[67]</sup> The single-atom IEIs contain donor/acceptor impurities. For Zn, for example, it is suggested that Zn–O pairs are produced with residual O impurities in Si substrates.<sup>[68]</sup> For Be, the IET is produced by Be–Be pairs.<sup>[69]</sup> For In, it is suggested that residual N atoms in Si substrates cause the IET formation.<sup>[59]</sup>

There are a relatively large number of papers on the Al–N IEI, and we utilized the Al–N IEI for our works. First, Weber et al. experimentally investigated emissions observed in Si:Al in detail; then, they suggested that the IETs in Si:Al were produced by a substitutional pair having  $C_{3v}$  symmetry along the  $\langle 111 \rangle$  axis.<sup>[70]</sup> Subsequently, Alt and Tapfer revealed that N atoms participate in these emissions,<sup>[71]</sup> and Modavis and Hall realized strong luminescence by the co-doping of Al and N.<sup>[67]</sup> Moreover, Tajima and Kamata utilized these emissions to estimate the residual N concentration in Si wafers.<sup>[72]</sup> The IET state is approximately 30 meV below the CBM.<sup>[70]</sup> The most recent studies were conducted by Iizuka and Nakayama using first-principles calculations.<sup>[73,74]</sup> They clarified the stable atomic configuration of the Al–N pair: the substitutional nearest-neighbor configuration is preferred over configurations comprising interstitials [Fig. 3(b)]. This configuration follows the prediction of Weber et al. based on their experiments. The Al–N pair provides a state in the band gap, which mainly comprises the N 3s state [Fig. 3(c)].<sup>[73]</sup>

### Proof-of-concept experiments On diodes

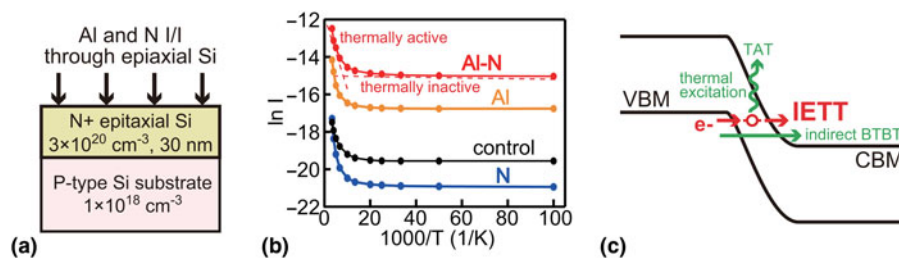
In this section, we discuss the enhancement of tunneling current flowing in diodes under the reverse-bias condition resulting from the introduction of an IEI, which was the first proof-of-concept experiment.<sup>[27,28]</sup> The diode consisted of an n-type epitaxial Si thin film on a p-type substrate [Fig. 4(a)]. The Al–N IEI was doped by the ion implantation (I/I) processes

and activated by low-temperature annealing at 450°C. The formation of the IET state was confirmed by photoluminescence spectroscopy at cryogenic temperature. The concentrations of Al and N were approximately  $10^{18} \text{ cm}^{-3}$  around the pn junction. Four types of diodes were examined: Al–N-, Al-, and N-implanted diodes and a control diode without additional impurities [Fig. 4(b)]. The temperature dependence of tunneling current in the control diode follows the trend of conventional indirect BTBT.<sup>[28]</sup> In the higher temperature range, the tunneling current flowing in the implanted diodes comprises the so-called trap-assisted tunneling (TAT) consisting of tunneling to an impurity or defect state and thermal emission from the state to the band. Therefore, it is fair to compare such currents with currents in the lower temperature range, in which tunneling consists of “pure” tunneling without thermal paths. In the comparison, the Al–N-implanted diode exhibited a current enhancement by a factor of 735, which implies that the Al–N co-doping enhances the tunneling current. The Al-implanted diode also exhibited current enhancement, but the enhancement was less than that in the Al–N case and is probably similar to the case of Tajima’s experiments,<sup>[72]</sup> in which the residual N impurity in a Si wafer causes the Al–N formation. The N-implanted diode exhibited no enhancement, but the current decreased because I/I defects are likely to compensate for carrier-generating dopants making the junction less steep. The current enhancement does not originate from the change of carrier concentration accompanying Al and N doping. The co-doping of Al and N induces hole generation in Si, and its activation ratio is approximately 10%.<sup>[75]</sup> Therefore, the change of carrier concentration does not significantly affect tunneling current.

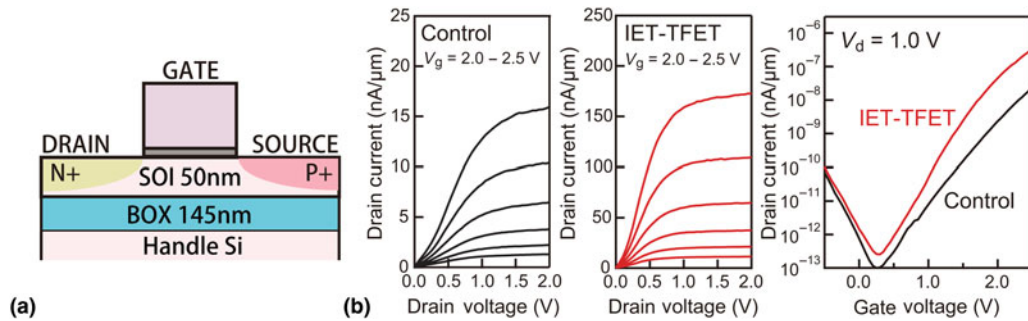
The above experiment was the first to show that the co-doping of Al and N enhances the tunneling current in Si. The supposed tunneling paths are summarized in Fig. 4(c). From this demonstration, it is not certain what IETT is—it will be discussed later with the results of a theoretical calculation.

### On TFETs

The next experiment was on TFETs,<sup>[27,76]</sup> which demonstrated N-type TFETs on a silicon-on-insulator (SOI) wafer. The



**Figure 4.** (a) Schematic representation of diodes fabricated in Refs. 27 and 28. (b) Temperature dependence of four types of diodes.<sup>[28]</sup> (c) Summary of tunneling paths in IET-assisted diodes.<sup>[28]</sup>



**Figure 5.** (a) Schematic representation of an N-type TFET fabricated on an SOI wafer.<sup>[27]</sup> (b)  $I$ - $V$  curves of the control TFET, which does not incorporate IET, and IET-TFET.<sup>[27]</sup>

high- $k$ /metal gate technology was also utilized [Fig. 5(a)]. The  $I$ - $V$  characteristics at room temperature are shown in Fig. 5(b). The  $I_d - V_d$  curves exhibit  $I_{ON}$  enhancement by a factor of 11 owing to the doping of Al-N. The SS was also improved owing to the current enhancement, as expected from Eq. (3). These improvements were also observed at a cryogenic temperature, as in the diode case. The  $I_{OFF}$  slightly increased because of the increase of tunneling current flowing through the junction at the drain side. This is not essential for the IET technology. If we utilize the so-called drain-offset structure,<sup>[77]</sup> we can avoid the  $I_{OFF}$  increase despite utilizing IET technology.<sup>[78]</sup> Unfortunately, the enhancement is less than that of diodes, which is supposed to be related to the mechanism of IETT, as discussed later. The entire active region consisting of the source, channel, and drain was exposed by Al-N I/I in the experiments. Then, the source sheet resistance was increased with I/I,<sup>[27]</sup> which suggests that Al-N implantations compensate for carrier-generating dopants, as is the case with N implantation in the diodes.

Another experiment has been conducted utilizing heated ion implantation (HII),<sup>[78]</sup> which is used to reduce implantation defects by heating the wafer when I/I is performed. In the experiment, the wafer was heated to 200°C in the Al and N implantation processes. The HII process realized an  $I_{ON}$  value three times that of the conventional IET-TFET with the RT I/I process. A lower number of I/I defects result in stronger IET effects. The comprehensive scenario is as follows. The defects hamper the IET activation. Fewer defects increase active IET and result in the greater current enhancement. It is supposed that the current enhancement with IET notably concerns the microscopic structure surrounding Al-N pairs.

### On TFET circuits

The final objective of  $I_{ON}$  enhancement is faster circuit operation. Complementary TFET (CTFET) circuit operation has been demonstrated with the IET technology.<sup>[29]</sup> The experiment was slightly different from the experiments in the previous section.  $I_{ON}$  enhancement by factors of five and two has been achieved in P- and N-type TFETs, respectively [Fig. 6(a)].

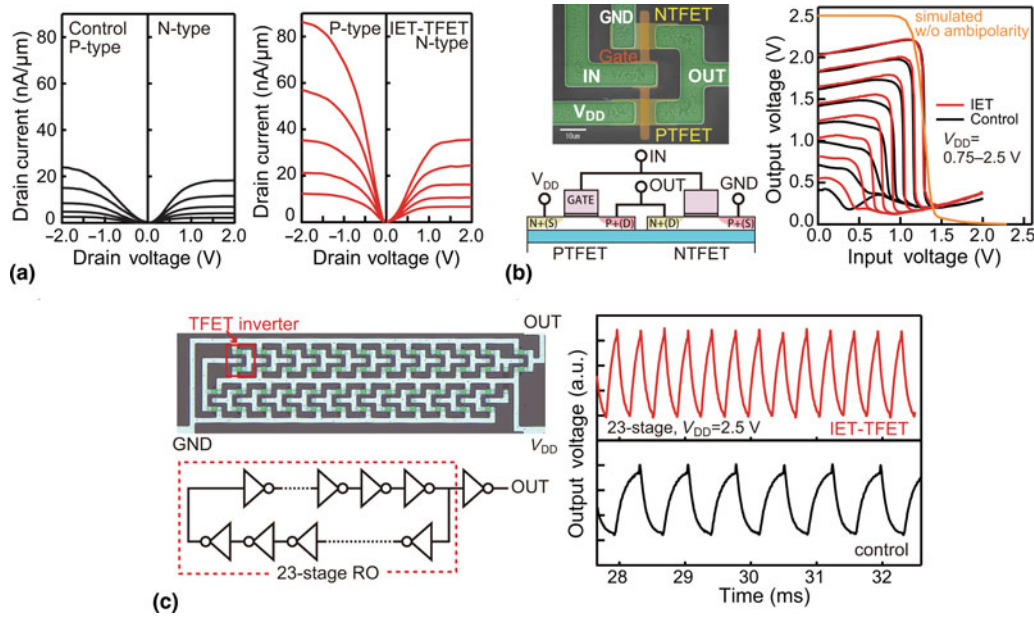
The simplest CTFET circuit is an inverter, as shown in Fig. 6(b). A higher gain was achieved, especially in a low operation-voltage range, owing to the  $I_{ON}$  enhancement. The full swing was not achieved because of the high  $I_{OFF}$ , which can be avoided by using the drain-offset structure simulated as an orange curve in Fig. 6(b). The situation seems to be the case in the previous section.

The ring oscillator (RO) circuit is fabricated to estimate circuit operation speed, which is the first performance indicator for newly developed devices. Twenty-three-stage full TFET ROs, in which all transistors were TFETs, were fabricated and successfully operated [Fig. 6(c)].<sup>[27]</sup> The output waveforms are also shown in the figure. It is clear that the IET technology enhances operation speed owing to the current enhancement. It is noted that this was the first demonstration of RO circuit operation for TFETs.

### Theoretical view of IETT

Iizuka et al. reported the theoretical framework of IETT.<sup>[79]</sup> This section is based on their paper. Figure 7(a) shows the tunneling path of IETT. Electron tunneling occurs in path A, which has a long distance. It is assumed that electrons move in path B by drift transport because the IET state resonates with the CB state. We find that the assumption is correct later. It is noted that IETT does not include thermal paths; therefore, it is expected that IETT exhibits no temperature dependence like TAT, which includes a thermal transition path. On the other hand, the experiments showed a temperature dependence of SS. It was probably caused by TAT originating from defects in the junction, which are not an essential characteristic of IETT.<sup>[27]</sup>

According to Eq. (1), we should first consider DOS. The DOS of the VBM and CBM were estimated as  $D_v = 1.19 \times 10^{10} \text{ eV}^{-1}$  and  $D_c = 8.16 \times 10^9 \text{ eV}^{-1}$ , respectively. In contrast, the DOS of the IET state was liberally estimated as  $D_{IET} = 3.25 \times 10^7 \text{ eV}^{-1}$  under the assumption that all Al and N atoms formed activated pairs in the host material. As  $D_{IET}$  is two orders of magnitude less than  $D_c$ ,  $|M|^2$  must compensate for the shortage to realize a higher current.

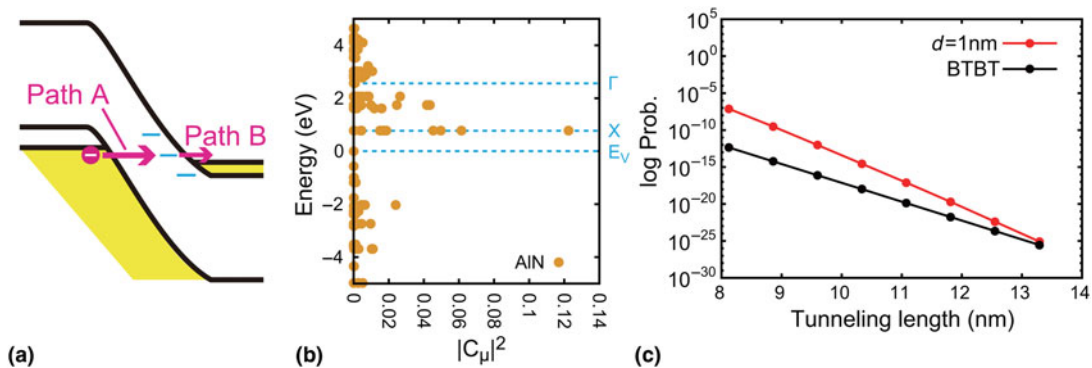


**Figure 6.** (a)  $I_D - V_D$  curves of P- and N-type TFETs. The IET technology enhances tunneling current.<sup>[29]</sup> (b) SEM image, schematic structure, and transfer curves of TFET inverters.<sup>[29]</sup> (c) Optical microscope image, schematic circuit diagram, and output waveforms of 23-stage full TFET ring oscillators.<sup>[29]</sup>

Two factors are involved in the enhancement of  $|M|^2$ . One is tunneling length. The effective tunneling length of IETT is the length of path A shown in Fig. 7(a), which is clearly shorter than the length of BTBT, resulting in a larger  $|M|^2$ . Here, we consider path B in which electrons move by drift transport as assumed in the first part of this section. Figure 7(b) shows a plot of components of  $\psi_{IET}$  decomposed by the wave functions of host Si as a function of eigenenergy. The IET state mainly comprises X-point-like states. This indicates that the IET state resonates with the CBM state of host Si, because of which path B does not contribute to tunneling and IETT takes advantage of the shorter tunneling length. The other factor is the relaxed  $k$ -conservation rule. Figure 7(b) also shows

that the variety of components is notably significant, which indicates that the IET state is localized and can relax the  $k$ -conservation rule along the tunneling direction. In relation to this, it is also important that the probability of BTBT in silicon is lower because of p-to-p transition as discussed previously, while the probability of IETT is higher because of p-to-s transition owing to the N-3s orbital nature of the IET state as discussed with Fig. 3(c). These two factors, tunneling length and relaxed  $k$ -conservation rule, enhance  $|M|^2$  to enhance tunneling current, despite the lower DOS.

Figure 7(c) shows the tunneling probability as a function of tunneling length. Both BTBT and IETT show the same trend of exponential increase with decreasing length. Here, we point out



**Figure 7.** (a) Tunneling of IETT consisting of two paths: the longer path A and the shorter path B. (b) Plot of components of  $\psi_{IET}$  decomposed by wave functions of host Si,  $\phi_{Si,\mu}$ , as a function of eigenenergy, where  $|C_{\mu}|^2 = |\langle \psi_{IET} | \phi_{Si,\mu} \rangle|^2$ .<sup>[79]</sup> (c) Tunneling probability of BTBT and IETT. The length of path B is assumed as  $d = 1$  nm.<sup>[79]</sup>

the difference of slope between these two curves. This difference is due to the difference of envelope function, and it indicates that a shorter tunneling length can realize a much higher enhancement ratio between IETT and BTBT. That is, if we realize a much shorter tunneling length—through device-structure modification, for example—we can expect a higher  $I_{ON}$  in Si-TFETs. Furthermore, it is speculated that this causes the difference of enhancement ratio between the diodes and TFETs in the experiments. This fact is notably promising for Si-TFETs because we can expect a higher  $I_{ON}$  than in the proof-of-concept experiments.

## Summary and future outlook

In summary, we reviewed the IET technology proposed to enhance  $I_{ON}$  in Si-TFETs. The proof-of-concept experiments demonstrated an  $I_{ON}$  enhancement in SOI-TFETs by a factor of approximately 10. Theoretical calculation predicts that it is possible to realize a much higher  $I_{ON}$  enhancement.

Here we comment on certain features of TFETs not mentioned in the main text. The fabrication process of Si-TFETs is compatible with that of conventional Si-MOSFETs; therefore, the fabrication cost does not matter. The scalability is expected to be better than that of MOSFETs because the short-channel effect is supposed to be insignificant in TFETs, the major characteristics of which are determined by the source-side edge of the gate. Therefore, in principle, planar-type TFETs could operate even in the technology node in which finFETs are utilized. The most important issue in the fabrication is source/drain formation because the self-alignment process of the source and drain for TFETs is not clear at present, which could hamper dimensional scaling. The performance variability is also under research. Especially for IET-TFETs, we can speculate that the IET impurities provide additional variation. On the other hand, it was reported that IET-TFETs exhibited less variation than conventional TFETs in the case of large devices, which is attributed to the decrease of tunneling rate fluctuation with the increase of tunneling probability.<sup>[76]</sup> Smaller IET-TFETs could exhibit much larger variation because of impurity fluctuation; however, there is a trade-off relationship between the increase of impurity fluctuation and the suppression of tunneling rate fluctuation. More research is needed to discuss the variability of IET-TFETs in detail.

Finally, we present an estimation of the future performance of IET-TFETs by utilizing simulations.<sup>[29]</sup> The enhancement in Si-TFET was assumed to be as high as in the case of the diodes; that is, enhancement by a factor of 735 was assumed. Here, not only  $I_{ON}$  enhancement but also threshold-voltage optimization and device miniaturization to reduce capacitance were considered. The target operation voltage is approximately 0.3 V, at which MOSFETs show subthreshold operation.<sup>[80]</sup> Here, MOSFETs operate with diffusion current, because of which mobility enhancement technologies to enhance drift current cannot be utilized. In this low operation-voltage range, IET-TFETs can be comparable or superior to 65-nm-node MOSFETs.

A similar prediction has been reported for III-V or Ge TFETs. These TFETs still have issues as P-type TFETs and in the device integration process. On the other hand, IET-TFETs are required to realize a much higher  $I_{ON}$  experimentally. Now, we have some types of TFETs as candidates for building blocks of low-power-consumption LSIs. Competition for device demonstrations with performance suitable for practical application is underway. At present, it is not certain which TFET is the best, but researchers are expected to usher in a new era of high-performance computers realized by new low-power-consumption transistors.

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