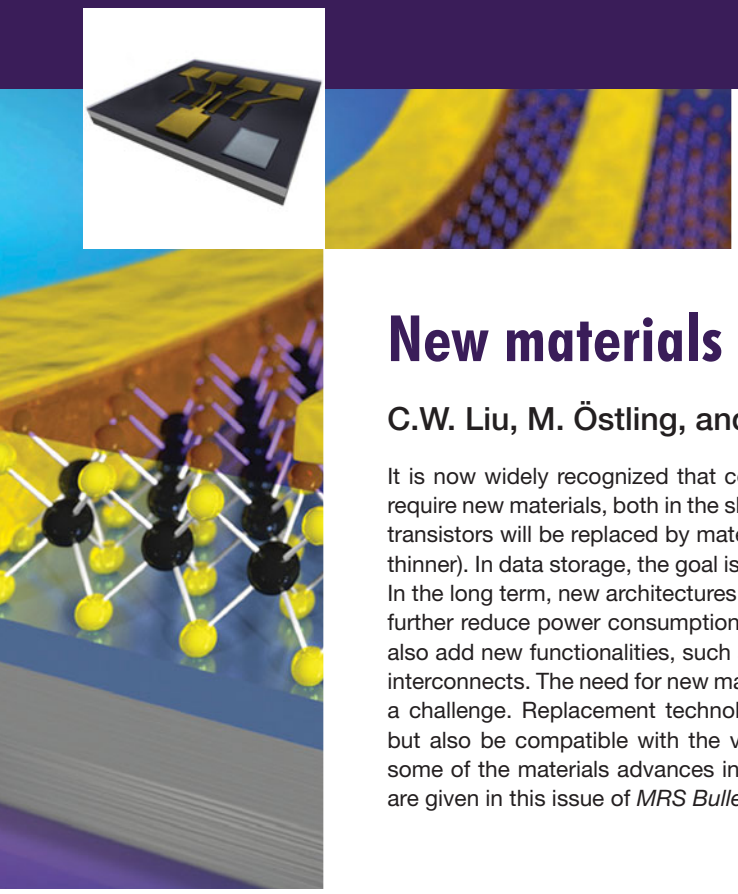

New materials for post-Si computing

C.W. Liu, M. Östling, and J.B. Hannon, Guest Editors

It is now widely recognized that continued performance gains in electronic computing will require new materials, both in the short and long term. In the short term, the silicon channel in transistors will be replaced by materials with higher mobility that are easier to "scale" (make thinner). In data storage, the goal is to have fast, non-volatile memory with a smaller cell size. In the long term, new architectures and new types of logic devices will be needed in order to further reduce power consumption. New materials cannot only boost performance, but can also add new functionalities, such as on-chip photonics, which can vastly improve interchip interconnects. The need for new materials is a big opportunity for materials research, but also a challenge. Replacement technologies must outperform conventional silicon technology, but also be compatible with the vast infrastructure of silicon manufacturing. Examples of some of the materials advances in the areas of computation, memory, and communication are given in this issue of *MRS Bulletin*.

Extension of Si CMOS

Up until the late 1990s, the performance gains implied by "Moore's Law"—the number of transistors on an integrated circuit doubles about every node—in microelectronics were achieved mainly through what is now called traditional scaling.[1] Roughly speaking, scaling corresponds to shrinking the device dimensions and supply voltage by a constant factor while leaving the materials unchanged.[2] The benefits of scaling are increased circuit density, faster devices, and lower power consumption. Note that the performance gains of traditional scaling are not predicated on improvements in materials properties (e.g., channel mobility and gate dielectric permittivity). They are mainly due to reduced capacitance and lower supply voltage. Unfortunately, we are now faced with the reality that fundamental materials limitations make traditional scaling of Si technology problematic. The consensus view is that continued performance improvement requires new materials, new device geometries, and new switching concepts.

Replacing Si with high-mobility channel materials (e.g., Ge/GeSn or III–V compounds) (**Figure 1**) is one near-term approach to improving performance (see the Gupta et al. article in this issue). However, replacing Si and SiO_2 is not a trivial task, and complex "integration" issues must be overcome. For example, the lattice mismatch between new channel materials and Si substrates can generate dislocations at the interface, which degrades performance and yield. To mitigate these effects, graded relaxed buffers,[3] dislocation removal,[4] and aspect ratio trapping[5] to reduce the dislocation density in active areas have all been explored. To date, the performance of these hybrid devices has not matched expectations.

For example, while bulk Ge has both high electron and hole mobility (Figure 1), Ge n-channel metal oxide semiconductor field-effect transistors (MOSFETs) do not exhibit the expected mobility enhancement as compared to Si MOSFETs. Currently, III–V (InGaAs) channels are more promising for NFETs. Ge and III–V materials have the appeal that they can be grown on a surface in a similar way as Si, which may make them easier to incorporate in a conventional processing flow. A more radical approach is to use novel one-dimensional (1D) (nanotubes, nanowires) or 2D (graphene, dichalcogenides) nanomaterials in place of conventional semiconductors. Because they are "small," these materials offer better electrostatic control of the channel, but their integration with conventional processing is potentially very difficult. Finally, devices such as the "tunnel FET" achieve high performance by incorporating new channel materials that enable device switching over a narrow voltage range, and hence with lower power. Moving away from conventional planar devices is another approach to improving performance. Better electrostatic control can be obtained if the gate "wraps around" the channel.

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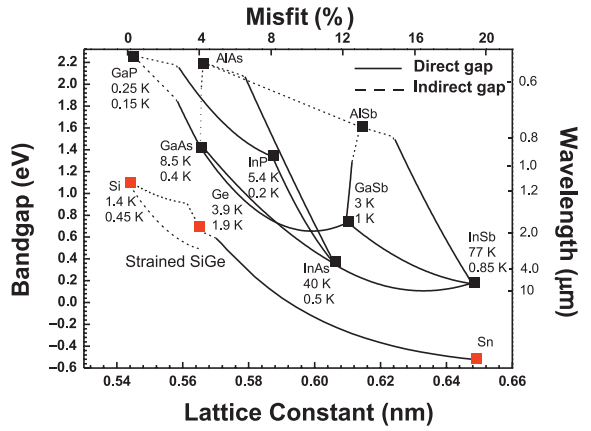

Figure 1. The plot of bandgap energy/wavelength versus lattice constant/misfit for III–V, Si/Ge/Sn. The numbers below the chemical symbols are electron and hole mobilities in units of cm^2/Vs. The solid lines indicate direct bandgaps.[25] (The red symbols are column IV elements.)

New device geometries such as tri-gate transistors and FinFETs shown in **Figure 2** accomplish this goal. Instead of a planar electrode, these devices have gate electrodes that surround the channel on three sides.

For high-performance devices, the figures of merit are high on-state current (I_{on}), low off-state current (I_{off}), and low supply voltage (V_{DD}) mainly to increase the chip speed, to decrease static power dissipation, and to decrease the dynamical power dissipation, respectively. To have high I_{on} and low I_{off} in the very narrow V_{DD} range, a small subthreshold slope (SS) ($SS = \left(\frac{d(\log_{10} I_{DS})}{dV_G}\right)^{-1}$) is required, where I_{DS} is the source-drain current and V_G is the gate voltage. This means the device can be turned on and off over a very small range of gate voltages. Classical thermionic transport imposes a theoretical lower bound of 60 mV/decade on the SS of MOSFETs. A gate stack with low equivalent oxide thickness (EOT) and low interfacial defect density (D_{it}) can push SS toward this theoretical value. It is possible to have SS smaller than 60 mV/dec by either using tunneling transport (tunneling FET or TFET) or adding a negative capacitor into the gate stack to obtain a voltage gain

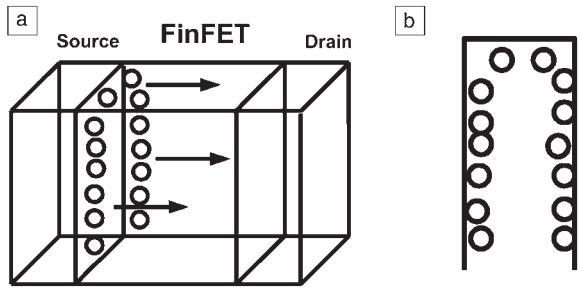

Figure 2. The schematic structure of FinFET/tri-gate transistors. (a) The 3D structure and (b) the cross-section of the channel. The circles represent charge carriers.

on the channel surface (negative capacitive FETs or NCFETs). However, TFETs[6] suffer from low I_{on} due to the low tunneling rate, and NCFETs[7] suffer from hysteresis due to the ferroelectric materials in the gate stack.

III–V compound semiconductors, Ge, and GeSn transistors

This group of post-Si materials is the most mature alternative to Si on the market, together with Ge-based technology. In the article by Riel et al. in this issue, a number of plausible III–V transistor structures are discussed. Not only traditional planar layouts but also several nanowire/3D architectures are described. The results in this area are very promising, and device performance can be substantially boosted. However, new technology comes at a high price. The key issue, besides the actual device and circuit processing, is the growth of compound materials on a Si platform and integration with conventional processing methods.

A recent review paper by Lourdudoss[8] gives an overview of a number of growth alternatives for III–V on Si. In addition to the direct transistor performance boost obtainable by implementing III–V technology, there is also a wide range of added functionality available in the integrated photonics arena.

While III–V devices appear to be good candidates for *n*-type FETs, Ge and GeSn appear to be superior for *p*-type FETs. The details are described in the article by Gupta et al. The improvement of D_{it} passivation/low EOT, doping concentration/activation, contact resistance, and surface roughness/mobility of Ge FETs is in progress and sheds light on Ge/GeSn complementary metal oxide semiconductor (CMOS) applications.

On-chip silicon photonics

Silicon photonics is the natural extension of Si electronic computing and storage. The integration of new materials, particularly of direct bandgap materials, enables wavelength tuning (see right axis of Figure 1). Monolithically integrated silicon photonics, including active devices and passive waveguides, with electronics offers a promising platform for scaling functionality (see the Kimerling et al. article in this issue). Waveguides, optical isolators, light sources, detectors, and modulators can all be integrated with conventional electronic devices. Ge is a promising material for both electronic and photonic devices due to its high carrier mobility and optical characteristics. The direct valley at the Γ point in reciprocal space (center of the zone) is only 140 meV above indirect valleys in the reciprocal L points (located at the edge of the Brillouin zone). The emission wavelength of the direct bandgap is around 1550 nm, which is useful for optical interconnects and telecommunication. To increase the direct band emission, *n*-type doping was used by the Kimerling group at MIT to boost the optical gain of Ge lasers,[9] which illuminates group IV photonics. Metal-insulator-semiconductor light-emitting diodes employing either Si[10] or Ge[11] as the active material, coupled with quantum waveguide structures, can cover the luminescence spectra from 1.1 μm to 2.2 μm.[12]

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The 3D stacking of integrated circuits using through-silicon via (TSV) technology can increase the bandwidth of interchip communications, both by shortening the travel distance and by providing a large number of I/O channels. However, when the bandwidth of an interconnect line increases beyond 10 GHz, the transmission efficiency is reduced. Photonic components can overcome this serious drawback. Heterogeneous integration of photonics and electronics on the 2.5 D interposer, which has many chips closely integrated on Si or other substrates, is an alternative to the heterogeneous integration of these components. Waveguide-integrated GHz GeSi electron-absorption modulator waveguides with ultralow energy consumption have been reported.[13] The efficient quantum-confined Stark effect in silicon-based structures by strained Ge multiple quantum wells has been demonstrated.[14] A photodetector using the metal-insulator-semiconductor tunneling structure operated in the deep depletion region can have infrared detection up to 10 μm.[15]

All spin logic

One of the key issues limiting the performance of scaled CMOS is the inability to reduce the supply voltage. As noted previously, part of this is related to the fundamental limits intrinsic to switching the current in a conventional FET. One way around this limitation is to use different state variables to store information. One rationale for pursuing alternate state variables is that the energy required to switch the device could be far less than in conventional Si technology. Behin-Aein et al. in this issue describe approaches in which information is stored in the orientations of small nanomagnets, so-called "all spin logic." In addition to low-power conventional computing, all spin logic could provide a pathway to practical non-Boolean computing schemes such as neural networks. Behin-Aein et al. describe spin-based computing both at the nanoscale, using nanomagnets, and at the atomic scale, by manipulating individual spins. They outline a nanoscale spin switch based on magnetic tunnel junctions, describe how spin information is programmed and read, and discuss the materials requirements for stability and data retention for 20 nm devices. They also review the potential for scaling, describing work in which atomic-scale logic operations were performed using the spin of individual magnetic atoms arranged on substrate.

Phase change memory

The most common memory technologies store information as charge. In the case of dynamic RAM (DRAM), this charge is stored on a capacitor. For the "flash" memory in the ubiquitous "thumb" drives, charge is stored on a floating gate. DRAM is used for computer memory because it is fast, but the capacitor charge must be periodically refreshed, making the memory volatile. In contrast, flash memory is slow, but the charge is retained without periodic refreshing. Both technologies are extremely robust and have been aggressively scaled. However, continued DRAM and flash scaling face many of the same issues that are anticipated for Si technology as a whole.[16,17] Uncertainties about the prospects for further scaling have spurred the search for new memory technologies that are not based on charge storage. These technologies could potentially offer a cheaper path to scaled (e.g., 10 nm), nonvolatile memory with fast read and write times. One of the most mature candidate technologies is phase change memory (PCM) (see the Raoux et al. article in this issue). Information in PCM is encoded in the crystal structure of the PCM cell, which can adopt either a low-resistance crystalline state or a high-resistance amorphous state. The state of the cell is

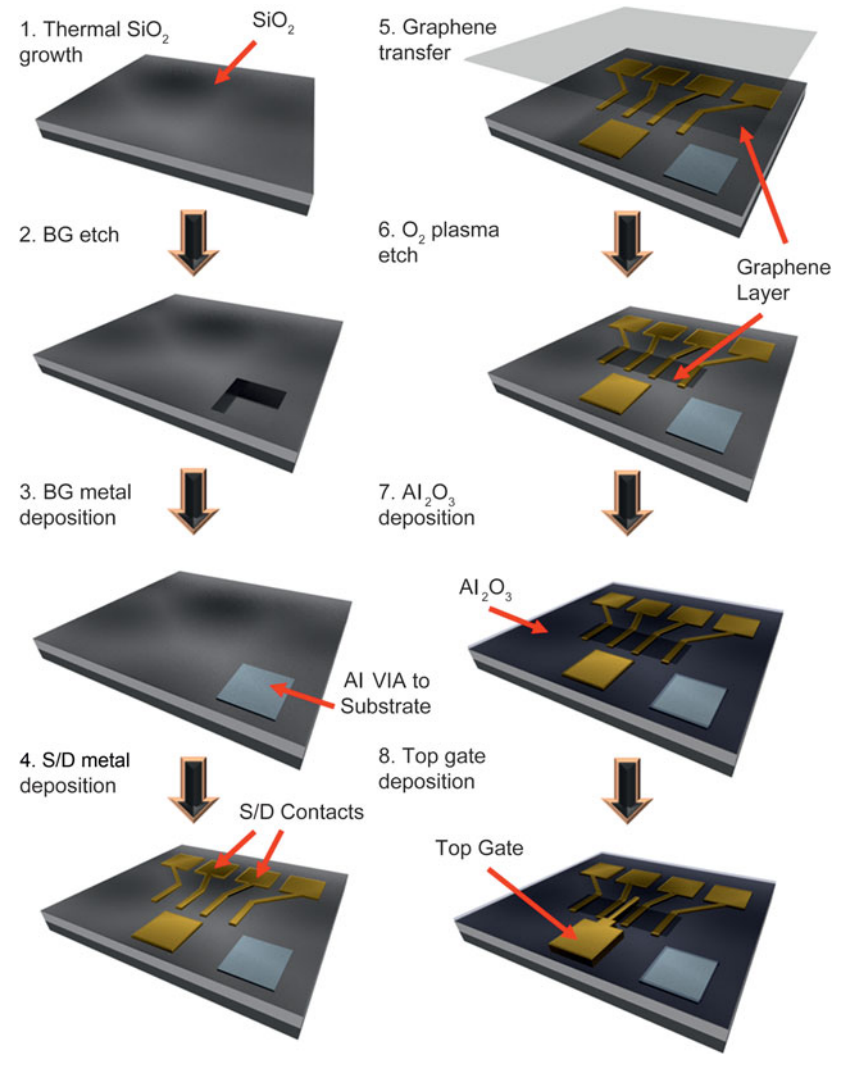

Figure 3. A typical wafer scale graphene transfer process. More details can be found in Reference 20. Note: S/D, source/drain; BG, back gate.

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changed by heating. The rate of cooling—fast for amorphous, slow for crystalline—determines the state of the cell. The state is read by measuring the resistance. One of the exciting prospects of PCM is that it could potentially scale to higher densities than DRAM.

Two-dimensional materials for electronic applications

Two-dimensional materials have received tremendous attention as replacement channel materials in Si nanoelectronics. Most of the interest is of course in graphene, the "Nobel" material studied by Novoselov and Geim in 2004,[18] who were awarded the Nobel Prize in 2010. In their article, Lemme et al. describe graphene's history and potential in detail and discuss future expectations of graphene technology, as well as the potential of other 2D materials in the group of transition metal dichalcogenides (TMD). Many alternative application areas are foreseen for this new group of materials, mainly by adding functionality to conventional CMOS. Huge research efforts are being invested in these material groups, the most notable being the "Graphene Flagship" program sponsored by the European Commission, with a tentative total budget of one billion Euros.

Despite the exciting possibilities of these novel materials, there are still fundamental manufacturing obstacles to be solved before they can have an impact on technology. One clear example is the integration of high-quality, large-area graphene with CMOS. Large domain graphene must be synthesized and transferred to a CMOS substrate without degrading the electrical properties.[19,20] An example of a proposed process flow for this is shown in **Figure 3**.

Carbon nanotube transistors

Recent improvements in device performance have come with the introduction of new materials and new device geometries. The use of carbon nanotubes (CNTs) as the channel material is an extreme example of this trend. In their article, Chen et al. describe the potential of CNT-based logic technology. In fact, CNTs may be the first "nanotechnology" to have a significant impact in high-performance logic technology. Because CNTs are small—with a diameter on the order of a nanometer—good electrostatic control of the channel is possible, even for extremely small devices (channel lengths below 10 nm).[21] In addition, CNT devices are inherently fast. CNTs have a true one-dimensional band structure with relatively high optical phonon energies. Consequently, inelastic scattering is suppressed, and carrier transport can be ballistic.

As shown by the detailed discussion in this issue by Chen et al., CNT circuit fabrication techniques have reached a level where complex circuits—even microprocessors—can be readily made. However, to create logic technology that outperforms conventional CMOS, serious integration challenges must be overcome. The most obvious hurdles are CNT purification and CNT placement from solution. CNT populations must be purified, because most synthesis methods produce a wide variety of CNTs. Conceptually, a CNT can be created by cutting a long strip out of a graphene sheet (or sheets) and joining the long edges, as shown in **Figure 4**. Differences in internal structure—and electronic properties—correspond to different orientations of the graphene strip. For example, roughly one-third of the CNTs produced using standard methods will be metallic. For transistor applications, these metallic CNTs must be completely eliminated. The placement problem is equally formidable. To build a microprocessor with minimal device variation, billions of CNTs must be placed at precise locations on a substrate, with a pitch on the order of 10 nm. Exciting progress has been made in recent years on both of these fronts.[22,23]

One important materials issue in CNT electronics concerns the electrical contacts. In most cases, contacts are made by depositing metal (e.g., Pd) onto the ends of the CNT while masking off the channel. Very little is known about the atomic structure of the contact or the factors that determine how electrons move from the metal to the CNT. Some insight can be gained by measuring how the resistance depends on the overlap length, L_c, of the metal and CNT (called the contact length). Franklin et al. showed that the contact resistance varies as $1/L_c$.[24] For the very short contacts needed for a scaled technology (on the order of a few tens of nm), the contact resistance is unacceptably high and must be improved in order for CNTs to be competitive.

Summary

The articles in this issue cover a wide range of emerging technologies for computation, communication, and storage. The ultimate success of these candidate technologies depends,

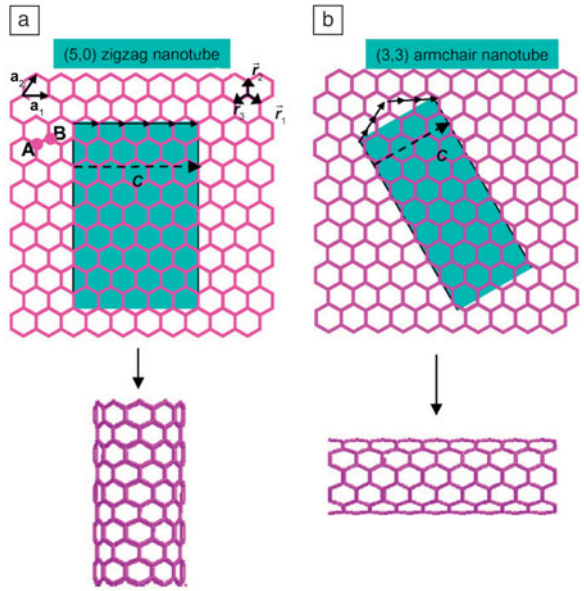

Figure 4. Single-wall carbon nanotubes can be formed by cutting strips from a graphene sheet (blue) and rolling them up such that each carbon atom is bonded to its three nearest neighbors. The creation of (a) "zigzag" and (b) "armchair" nanotubes are shown. A and B indicate the two carbon sublattices in the graphene structure. $\mathbf{a}_1$ and $\mathbf{a}_2$ are the graphene lattice vectors, and $\boldsymbol{C}$ is the so-called roll-up vector.[26]

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in large part, on materials innovations. For some, such as all-spin logic, progress depends on identifying new materials with superior intrinsic properties, for example, long spin diffusion length and high carrier mobility. For others, such as III–V compounds, graphene, and carbon nanotubes, the superior properties are well established; here, the challenge is integration. Specifically, new approaches in deposition, patterning, doping, and passivation are needed to make these new materials compatible with the existing manufacturing infrastructure. And for all cases, a deeper understanding of the physics at the nanoscale is needed to control doping, reduce contact resistance, limit leakage current, and improve the stability (retention time) of nanoscale memory elements.

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