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Avoiding the Curtaining Effect: Backside Milling by FIB INLO

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The introduction of the focused ion beam (FIB) instrument for site-specific material removal continues to alter the course of materials characterization. However, one of the disadvantages to FIB specimen preparation is what is commonly known as "curtaining." Curtaining artifacts are most often observed in semiconductor materials where multiple patterned layers of materials having a low sputtering yield blocks a faster sputtering yield material. In a bright field TEM image, curtaining appears as mass/thickness contrast where, e.g., the Si substrate appears darker under a gate than far from the gate. This artifact can be especially problematic in electron holography of semiconductor gate structures where the phase image is dependent on specimen thickness as well as the desired dopant distribution [1,2]. To eliminate curtaining effects, and hence, local differences in specimen thickness in the region of interest (i.e. the gate region of a semiconductor device), a technique based on in-situ lift-out (INLO) was used to prepare semiconductor devices from the Si -side of the device. Backside milling by FIB INLO on an FEI single beam 200TEM FIB is described below.

FIG. 1 shows an in-situ probe just touching a piece of material FIB milled free for subsequent lift-out. Note that the Si substrate is located on the side opposite the probe. In FIG. 2 the probe is positioned such that is comes through the opening of a slotted Cu grid. The specimen is mounted on the side of the Cu grid using ion beam assisted Pt deposition. A low magnification FIB image of the specimen mounted on the Cu grid after the probe has been removed is shown in FIG. 3. Note that the Cu grid was cut prior to mounting it in the specimen holder such that the cut faced downward in the specimen mount. The specimen mount was then removed from the FIB instrument and the Cu grid was flipped 180^{o} such that the grid cut now faced upwards. The holder was placed back into the FIB such that FIB milling could now be performed from the Si side of the specimen. Gate structures in the specimen were located and material below the gate (as viewed from FIG. 4) was removed by either (i) tilting to 54^{o}, FIB milling the material away, tilting back to 0^{o}, rotating 180^{o}, and repeating or (ii) after the specimen was mounted as in FIG 3, the specimen was re-mounted such that the plane of the Cu grid would be perpendicular to the beam to facilitate material removal below the gate. The specimen was FIB milled from the Si side directly to a thickness of ~ 300 nm for electron holograph. Alternatively, the specimens were FIB milled to ~ 800 nm and then further thinned in an ion mill in an attempt to remove FIB damage [3].

FIG. 5 shows a phase image of a PMOS device and FIG. 6 shows a phase image of an NMOS device. Note that FIGS 4,5,6 show no evidence of curtaining. Also evident in FIGS. 5 and 6 are the signature phase contrasts from the respective p-type (dark grey) and n-type (light grey) which outline the doped junctions. More details on the phase images appear elsewhere in these proceedings [3]. Thus, backside milling FIB INLO may be used to prepare uniformly thick specimens for subsequent electron holography analysis [4].

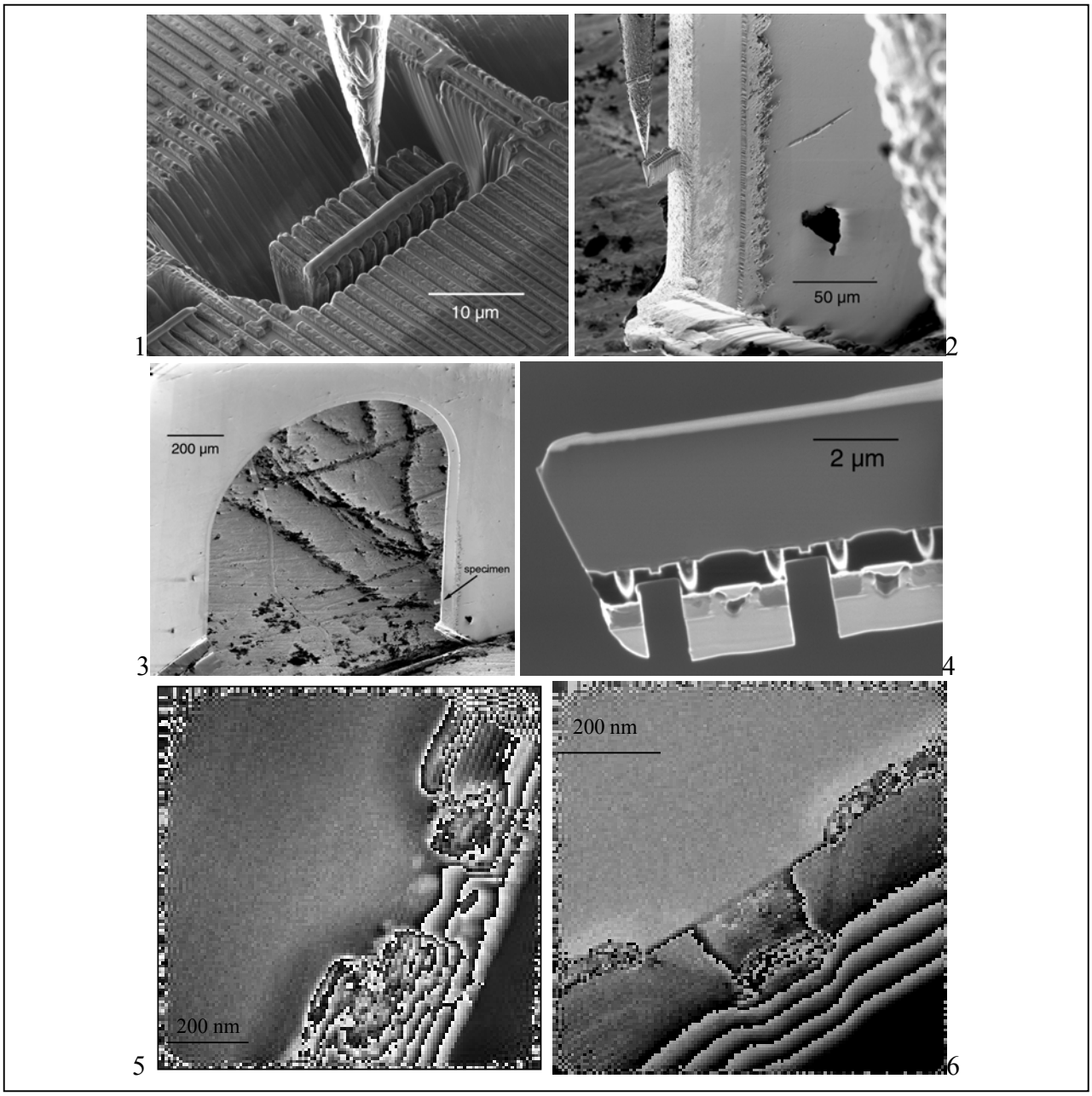

FIG 1. FIB image demonstrating INLO of a semiconductor device.
FIG 2. FIB image of the specimen mounted on the side of a Cu grid.
FIG 3. Low magnification FIB image showing the mounted specimen and grid.
FIG 4. FIB image showing the specimen FIB milled from the Si side (after flipping the grid 180^{o}).
FIG 5. Phase image of PMOS device prepared by backside FIB INLO.
FIG 6. Phase image of NMOS device prepared by backside FIB INLO.

References
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[3] Samples were obtained from SEMATECH. Thanks to FEI Company and Omniprobe for their support.